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Space product assurance

Qualification of printed circuit boards

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Foreword

This Standard is one of the series of ECSS Standards intended to be applied together for the management, engineering and product assurance in space projects and applications. ECSS is a cooperative effort of the European Space Agency, national space agencies and European industry associations for the purpose of developing and maintaining common standards.

Requirements in this Standard are defined in terms of what shall be accomplished, rather than in terms of how to organize and perform the necessary work. This allows existing organizational structures and methods to be applied where they are effective, and for the structures and methods to evolve as necessary without rewriting the standards.

The formulation of this Standard takes into account the existing ISO 9000 family of documents.

This Standard has been prepared by the ECSS Q-70-10 Working Group, reviewed by the ECSS Technical Panel and approved by the ECSS Steering Board.

This Standard is based on ESA PSS-01-710, CNES/QFT/SP. 0117, CNES/QFT/SP. 0118, CNES/QFT/SP. 0119, CNES/QFT/SP. 0120 (draft).

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Introduction

PCBs are used for the mounting of components in order to produce printed board assemblies performing complex electrical functions. The PCBs are subjected to thermal and mechanical shocks during their assembly such as mounting of components by soldering, rework and repair under normal terrestrial conditions, and in addition the complex printed board assembly are subjected to the environment imposed by launch and space flights.

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Scope

This Standard defines the basic requirements for evaluation, qualification and maintenance of qualification of space PCB suppliers for different types of printed circuit boards.

This Standard is applicable to the following type of boards:

- rigid printed boards (single-sided, double-sided, multilayer, sequential- laminated multilayer and metal core);
- flexible printed boards (single-sided and double-sided);
- rigid-flex printed boards (multilayer and sequential-laminated multilayer);
- high frequency printed boards;
- special printed boards.

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Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this ECSS Standard. For dated references, subsequent amendments to, or revisions of any of these publications do not apply. However, parties to agreements based on this ECSS Standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references the latest edition of the publication referred to applies.

ECSS-P-001	Glossary of terms
ECSS-Q-20	Space product assurance — Quality assurance
ECSS-Q-20-09	Space product assurance — Nonconformance control system
ECSS-Q-70	Space product assurance — Material, mechanical parts and processes
ECSS-Q-70-02	Space product assurance — Thermal vacuum outgassing test for the screening of space materials
ECSS-Q-70-08	Space product assurance — The manual soldering of high-reliability electrical connections
ECSS-Q-70-11	Space product assurance — Procurement of printed circuit boards
ECSS-Q-70-21	Space product assurance — Flammability testing for the screening of space materials
ECSS-Q-70-22	Space product assurance — The control of limited shelf-life materials
ECSS-Q-70-29	Space product assurance — The determination of offgassing products from materials and assembled articles to be used in a manned space vehicle crew compartment
IEC 60068-2-3 (1969-01)	Environmental testing. Part 2: Tests. Test Ca: Damp heat, steady state
IEC 60068-2-14-am 1 (1986-01)	Environmental testing. Part 2: Tests. Test N: Change of temperature

IEC 60068-2-20-am 2 (1987-01)	Environmental testing. Part 2: Tests. Test T: Soldering
IEC 60249-1-am 4 (1993-05)	Base materials for printed circuits. Part 1: Test methods
IEC 60326-2-am 1 (1992-06)	Printed boards. Part 2: Test methods
IEC 60326-5-am 1 (1989-10)	Printed boards. Part 5: Specification for single and double sided printed boards with plated-through holes
IEC 60326-8 (1981-01)	Printed boards. Part 8: Specification for single and double sided flexible printed boards with through connections
IEC 60326-11 (1991-03)	Printed boards. Part 11: Specification for flex-rigid multilayer printed boards with through connections
IEC 62326-4 (1996-12)	Printed boards. Part 4: Rigid multilayer printed boards with interlayer connnections – Sectional specification
IPC-4101	Specification for base materials for rigid and multilayer printed boards
MIL-P-50884C	Printed wiring, flexible and rigid-flex

3

Terms, definitions and abbreviated terms

3.1 Terms and definitions

The following terms and definitions are specific to this Standard in the sense that they are complementary or additional to those contained in ECSS-P-001.

3.1.1
blister
delamination in the form of a localized swelling and separation between any of the layers of a lamination base material, or between base material and conductive foil or protective coating

[IEC 60194 (1999-04)]

3.1.2
cover lay (flexible circuit)
the layer of insulating material that is applied covering totally or partially over a conductive pattern on the outer surfaces of a printed board

[IEC 60194 (1999-04)]

3.1.3
crazing
an internal condition that occurs in reinforced base material whereby glass fibres are separated from the resin at the weave intersections

NOTE 1 This condition manifests itself in the form of connected white spots or crosses that are below the surface of the base material. It is usually related to mechanically induced stress.

NOTE 2 See also “measling”.

[IEC 60194 (1999-04)]

3.1.4
delamination
a separation between plies within a base material, between base material and a conductive foil, or any other planar separation with a printed board (see also “Blister”)

[IEC 60194 (1999-04)]

3.1.5
dewetting
a condition that results when molten solder coats a surface and then recedes to leave irregularly-shaped mounds of solder that are separated by areas that are covered with a thin film of solder and with the basis metal not exposed

[IEC 60194 (1999-04)]

3.1.6
flexible printed board
a printed board either single, double sided or multilayer consisting of a printed circuit or printed wiring using flexible base materials only *[IEV 541-04-03, modified]*

[IEC 60194 (1999-04)]

3.1.7
haloing
mechanically-induced fracturing or delamination, on or below the surface of a base material, that is usually exhibited by a light area around holes or other machined features

[IEC 60194 (1999-04)]

3.1.8
high frequency printed board
printed board used for high frequency applications, that has specific requirements for the dielectric properties of the base laminates as well as special dimensional requirements for the lay-out for electrical purposes

3.1.9
inclusions
foreign particles, metallic or non-metallic, that may be entrapped in an insulating material, conductive layer, plating, base material or solder connection

[IEC 60194 (1999-04)]

3.1.10
key personnel
personnel with specialist knowledge responsible for defined production or product assurance areas

3.1.11
measling
a condition that occurs in laminated base material in which internal glass fibres are separated from the resin at the weave intersection

NOTE 1 This condition manifests itself in the form of discrete white spots or “crosses” that are below the surface of the base material. It is usually related to thermally-induced stress.

NOTE 2 See also “crazing”

[IEC 60194 (1999-04)]

3.1.12
metal core printed board
printed board using a metal core base material *[IEV 541-04-03]*

[IEC 60194 (1999-04)]

3.1.13
multilayer printed board
the general term for a printed board that consist of rigid or flexible insulation materials and three or more alternate printed wiring and/or printed circuit layers that have been bonded together and electrically interconnected

[IEC 60194 (1999-04)]

3.1.14
prepreg
a sheet of material that has been impregnated with a resin and cured to an intermediate stage, i.e. B-staged resin

[IEC 60194 (1999-04)]

3.1.15
printed board
the general term for completely processed printed circuit and printed wiring configurations

NOTE This includes single-sided, double sided and multilayer boards with rigid, flexible, and rigid-flex base materials. *[IEV 541-04-03, modified]*

[IEC 60194 (1999-04)]

3.1.16
printed circuit board
printed board that provides both point-to-point connections and printed components in a predetermined arrangement on a common base

[IEC 60194 (1999-04)]

3.1.17
rigid double-sided printed board
double-sided printed board, either printed circuit or printed wiring, using rigid base materials only *[IEV 541-04-03, modified]*

[IEC 60194 (1999-04)]

3.1.18
rigid-flex printed board
a printed board with both rigid and flexible base materials

[IEC 60194 (1999-04)]

3.1.19
rigid-flex double-sided printed board
double-sided printed board, either printed circuit or printed wiring, using combinations of rigid and flexible base materials

[IEC 60194 (1999-04)]

3.1.20
rigid-flex multilayer printed board
multilayer printed board, either printed circuit or printed wiring, using combinations of rigid multilayer and flexible single and double-sided base materials

3.1.21
rigid printed board
a printed board using rigid base materials only *[IEV 541-04-03, modified]*

[IEC 60194 (1999-04)]

3.1.22
rigid single-sided printed board
single-sided printed board, either printed circuit or printed wiring, using rigid base materials only *[IEV 541-04-03, modified]*

[IEC 60194 (1999-04)]

3.1.23
rigid multilayer printed board
multilayer printed board, either printed circuit or printed wiring, using rigid base materials only *[IEV 541-04-03, modified]*

[IEC 60194 (1999-04)]

3.1.24
scratch
a narrow furrow or grove in a surface

NOTE It is usually shallow and caused by the marking or rasping of the surface with a pointed or sharp object.

[IEC 60194 (1999-04)]

3.1.25
sequentially laminated multilayer printed board
a multilayer printed board that is formed by laminating together through hole plated double-sided or multilayer boards

NOTE Thus, some of its conductive layers are interconnected with blind or buried vias.

[IEC 60194 (1999-04)]

3.2 Abbreviated terms

The following abbreviated terms are defined and used within this Standard.

Abbreviation	Meaning
n.a.	not applicable
NRB	nonconformance review board
PCB	printed circuit board
PID	process identification document
PTH	plated-through hole
PTFE	polytetrafluoroethylene
r.m.s.	root-mean-square
TBD	to be defined

4

General

This Standard details the steps to obtain from the customer the qualification for supplying PCBs of an identified technology.

These steps are:

a. Evaluation;

b. Qualification:
   - Test and inspections,
   - Qualification approval;

c. Maintenance of qualification.

The supplier shall have or implement a quality assurance programme compatible with ECSS-Q-20.

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Evaluation

5.1 General

The PCB supplier who seeks qualification of his PCB manufacturing line shall:

a. request an evaluation;

b. supply evaluation printed boards;

c. submit to a manufacturing line audit.

If the result is satisfactory, the customer can authorize the go-ahead of the qualification test programme for each of the technologies that have been accepted.

5.2 Request for evaluation

The supplier's request for evaluation shall contain detailed description of the technology that they wish to be evaluated for. Further it shall contain a brief description of the manufacturing line, as well as details of past experience. Applications shall be signed by the person responsible for production and product assurance and shall be addressed to the customer.

5.3 Evaluation printed board samples

The supplier shall manufacture three PCB samples of each technology with the materials, processes and equipment that are intended for use in subsequent production for the customer. The PCBs shall represent the highest capability for which the supplier seeks approval and as far as possible conforming to this Standard.

The evaluation samples may be examined at an independent certified test house. The evaluation test performed shall be in accordance with the parameters shown as an example in annex B. The dimension of the samples shall be sufficient to contain a pattern enabling all of the listed inspections to be carried out for constructional analysis.

5.4 Line audit

Provided the evaluation samples are acceptable, the customer shall audit the manufacturing line when PCB production is in progress. Before or during the audit, the supplier shall make the following documents available to the customer:

a. Company organigram related to PCB production and control, including names and functions of all key personnel involved (as defined in this Standard).

b. Complete identification of the parameters of the technologies that they wish to qualify.

c. List of materials and equipment (including types and names of suppliers) used for production of PCBs.

d. List of process and control specifications with number, issue number, and date of issue or process identification document (PID).

e. Production flow-chart, including quality-assurance inspection point and relevant process specification.

f. Outline of test capabilities (e.g. equipment for metallographic examination, chemical analysis, failure analysis, mechanical and electrical test including functional testing of PCBs).

6

Qualification

6.1 General

After successful evaluation and before the start of the qualification sequence the PCB supplier shall submit a qualification test programme for approval. The test programme shall conform to this clause and clause 7.

The submitted qualification test programme shall show the key personnel involved, the test houses, the proposed schedule of test and submittal of final results as required in 13.1.

The customer may witness important tests.

6.2 Qualification sequence

6.2.1 Qualification steps

a. Qualification programme.
b. Definition of test boards.
c. Manufacturing of test boards.
d. Supply of test board.
e. Performance of test programme.
f. Qualification test review.
g. Qualification approval.

6.2.2 Qualification test programme

a. The qualification test programme shall be performed on test boards as described in 6.3.
b. The test boards shall be as defined in 6.4.1 and as agreed after evaluation, see clause 5.
c. The test boards shall be supplied to ECSS-Q-70-11.
d. Performance of test programme shall be decided according to subclauses 6.3. and 6.4.
e. Qualification test review see subclause 6.5.
f. Qualification approval, see clause 13.

6.2.3 Qualification testing

Qualification testing shall be performed in the following cases:

a. Initial qualification.

b. When qualification took place more than two years previously and maintenance of qualification was not assured.

c. New process technology was introduced (changes in base material, PCB structuring or chemical products requiring changes in chemical or mechanical processing parameters).

d. The production line was moved to another location.

e. Changes in key personnel (personnel with specialist knowledge responsible for defined production or product assurance areas).

6.3 Qualification test programme

6.3.1 Execution

The qualification test programme shall be executed in accordance with the test sequence, methods and requirements specified in Figure 1 and Table 1 on test specimens as described in subclause 6.4.

6.3.2 Test sequence

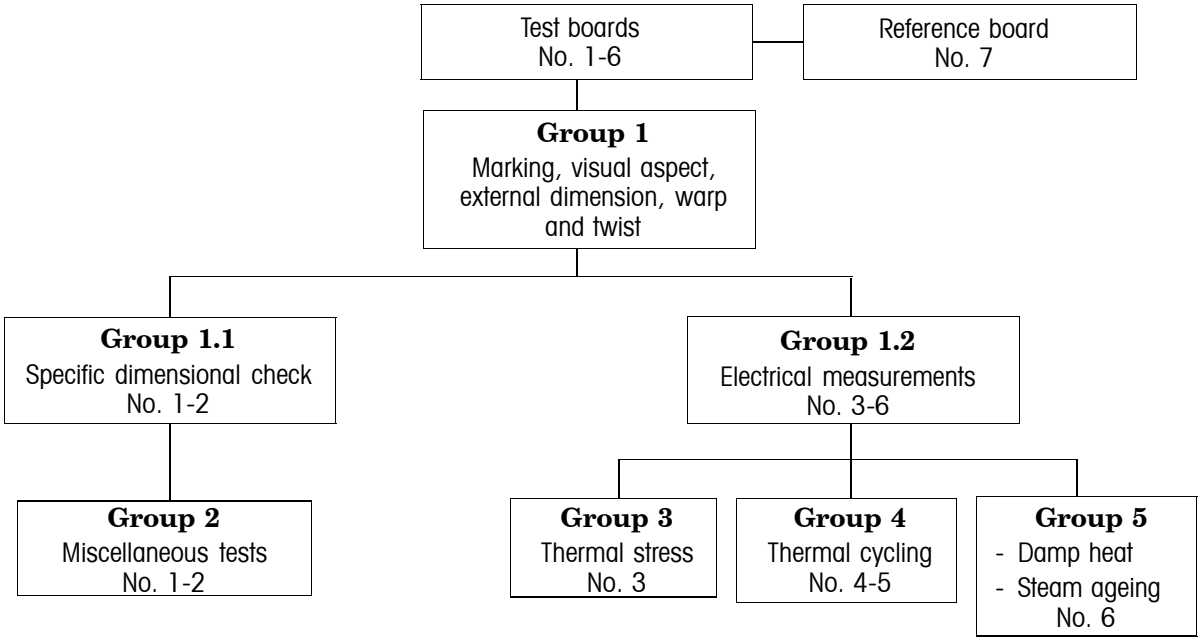


Figure 1: Qualification test flow chart

6.3.3 Test programme

Table 1: Test programme

Group	Tests	Test procedure	
		Methods and requirements clause or subclause	**Board no. Test specimen no.**
Group 1	**Initial test**	8	Boards 1-6
Subgroup 1.0	Visual inspection and non-destructive tests: - marking - visual aspect - external dimensions - warp - twist	8.1 8.1.1 8.1.2 8.1.3 8.1.4 8.1.5	Boards 1-6
Subgroup 1.1	Specific dimensional check	8.2	Boards 1-2
Subgroup 1.2	Electrical measurements: - intralayer [a] insulation resistance - interlayer [b] insulation resistance - dielectric withstanding voltage: • intralayer • interlayer - continuity - interconnection resistance - impedance test - dielectric constant and loss tangent for high frequency	8.3 8.3.1 8.3.2 8.3.3 8.3.4 8.3.5 8.3.6 8.3.7	Boards 3-6 Specimen A Specimen H Specimen A Specimen H Specimen D Specimen E Specimen Y Specimen W
Group 2	**Miscellaneous tests**	9	Boards 1-2
Subgroup 2.1	Solderability test: - wettability - microsectioning (option)	9.1 9.1 9.3.3	 Specimen J Specimen J
Subgroup 2.2	Mechanical tests: - peel strength - pull-off strength - resistance to bending cycles (for flexible PCBs) - bending test for rigid-flex	9.2 9.2.1 9.2.2 9.2.3 9.2.4	 Specimen B Specimen B Specimen X
Subgroup 2.3	Coating tests: - coating adhesion (for non-fused SnPb, Au and Au/Ni finishes) - coating analysis - microsectioning	9.3 9.3.1. 9.3.2 9.3.3	 Specimen G Specimen G Specimen F

Table 1: Test programme *(continued)*

Group	Tests	Test procedure	
		Methods and requirements clause or subclause	**Board no. Test specimen no.**
Subgroup 2.4	Electrical tests:	9.4	
	- current overload:	9.4.1	Specimen E
	• short time		
	• long time		
	- internal short circuit	9.4.2	Specimen C
Subgroup 2.5	Physical tests:	9.5	Specimen K
	- water absorption	9.5.1	
	- outgassing	9.5.2	
Group 3	**Thermal stress**	10	Boards 3
	Solder bath float and vapour phase solder simulation	10.2	Board (without specimen F)
	- substrate aspect test	8.1.2	Board
	- peel strength	9.2.1	Specimen B
	- continuity	8.3.4	Specimen D
	- interconnection resistance	8.3.5	Specimen E
	- microsectioning	9.3.3	Specimen J
	Rework simulation	10.3.	Specimen F
	- microsectioning	9.3.3	Specimen F
Group 4	**Thermal cycling**	11	Board 4-5
	- substrate aspect test	8.1.2	Boards
	- peel strength	9.2.1	Specimen B
	- continuity	8.3.4	Specimen D
	- interconnection resistance	8.3.5	Specimen E
	- intralayer insulation resistance	8.3.1	Specimen A
	- interlayer insulation resistance	8.3.2	Specimen H
	- dielectric withstanding voltage:		
	• intralayer	8.3.3	Specimen A
	• interlayer	8.3.3	Specimen H
	- microsectioning	9.3.3	Specimen F

Table 1: Test programme *(continued)*

Group	Tests	Test procedure	
		Methods and requirements clause or subclause	**Board no. Test specimen no.**
Group 5	**Damp heat — Steam ageing**	12	Board 6
	Damp heat	12.1	Board (without specimen F)
	– peel strength	9.2.1	Specimen B
	– intralayer insulation resistance	8.3.1	Specimen A
	– interlayer insulation resistance	8.3.2	Specimen H
	– dielectric withstanding voltage:		
	• intralayer	8.3.3	Specimen A
	• interlayer	8.3.3	Specimen H
	– microsectioning (if required)	9.3.3	Specimen F
	Steam ageing	12.2	
	– Solderability test:		
	• wettability	9.1	Specimen F
	– microsectioning (if required)	9.3.3	Specimen F

[a] i.e.: in the same layer.

[b] i.e.: between opposite layers.

6.4 Qualification test board

6.4.1 General

The qualification test board shall consist of a board of the highest complexity for which the supplier seeks capability approval for use in the space project. This test board shall consist of a capability specimen together with test specimens. The layout- of the test specimens shall be as described below. The layout of the capability specimen shall be agreed between customer and supplier and can be an actual PCB circuit to be used in the space project.

The test specimen design shall be in accordance with subclause 6.4.3 and the referenced IEC specification when in existence.

- Specification for single and double sided printed boards with plated-through holes (IEC 60326-5).
- Rigid multilayer printed circuit boards with interlayer connections (IEC 62326-4).
- Specification for single and double sided flexible printed boards with through connections (IEC 60326-8).
- Specification for flex-rigid multilayer printed circuit boards with through connections (IEC 60326-11).
- Sequentially laminated multilayer printed circuit boards.
- Special printed circuits boards to be defined between customer and supplier.

6.4.2 Location of test specimens and capability specimen

An example of a qualification test board layout for a rigid multilayer board is shown in Figure 2. A similar layout may be used for other types of boards.

6.4.3 Qualification specimen design

- The individual test specimens shall represent the grade of capability of the product.
- Individual test specimens are designed to evaluate specific characteristics of the PCBs they represent.
- The normative design of test specimens shall be in accordance with the IEC specifications.
- If the supplier wishes to demonstrate the product capability by using the qualification specimen (IEC term "capability test boards"), adequate multiple arrangement for test specimens may be used (see subclause 6.4.2) as an example.

  The pattern drawing on layer 1 of the individual test specimens given below and shown as an example in Figure 2 shall preferably be used.

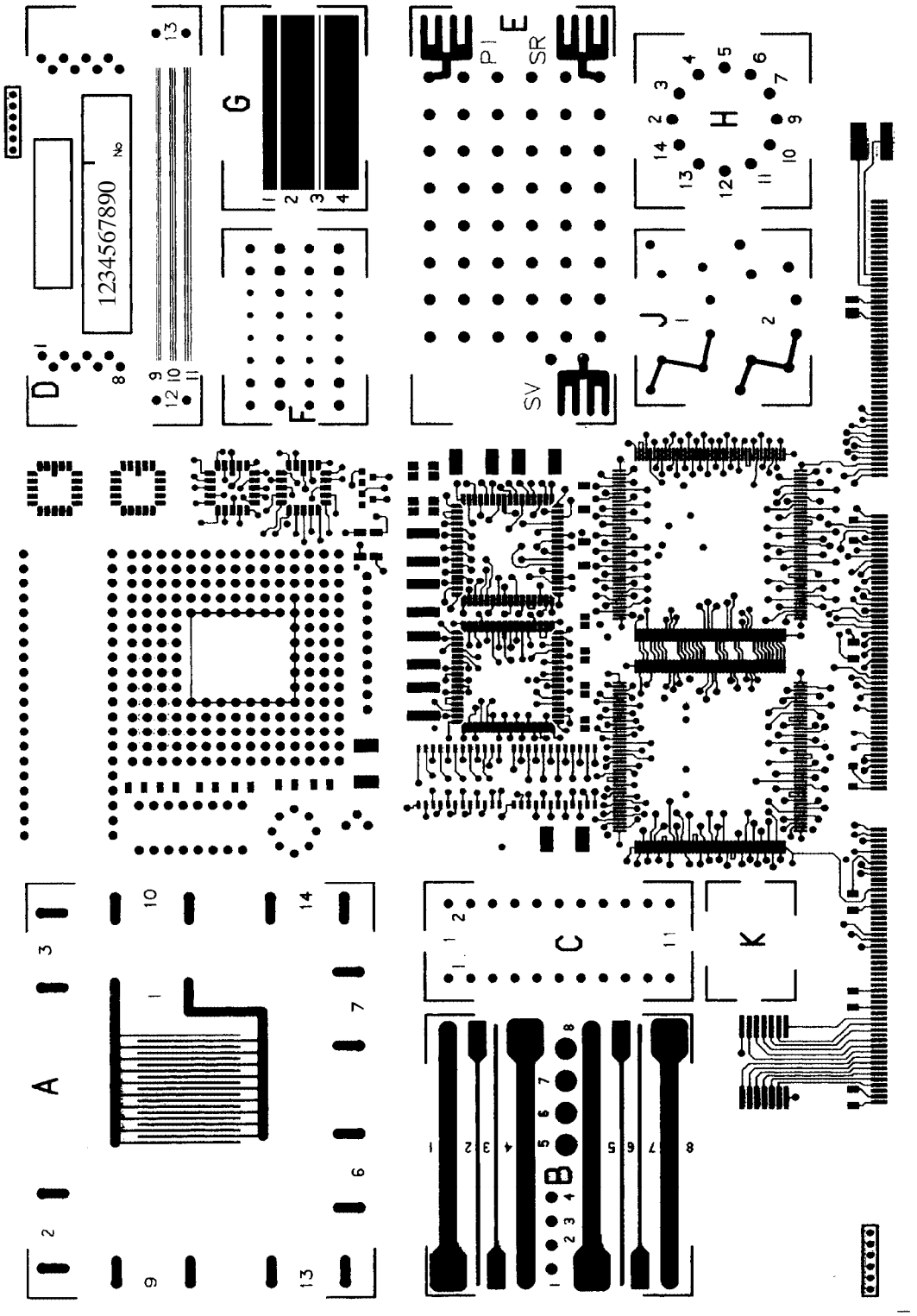


Figure 2: Example of a qualification test board layout with test specimens and capability specimen

6.4.3.1 Test specimen A: Electrical test

a. Intralayer insulation resistance.

b. Dielectric withstanding voltage.

For an example of a test specimen A see Figure 3.

Capability for all types of PCBs

- The conductor widths and spacing of each layer shall be the minimum used on the layer that is intended to be represented.
- The comb pattern can provide a useful tool for evaluating cleanliness.

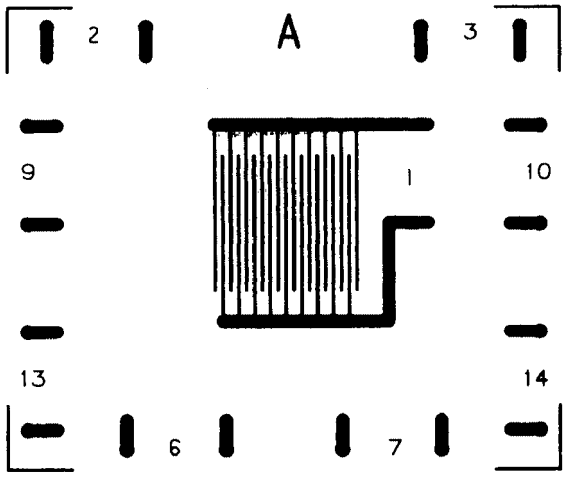


Figure 3: Example of test specimen layout for intralayer insulation resistance and dielectric withstanding voltage testing

6.4.3.2 Test specimen B: Mechanical test

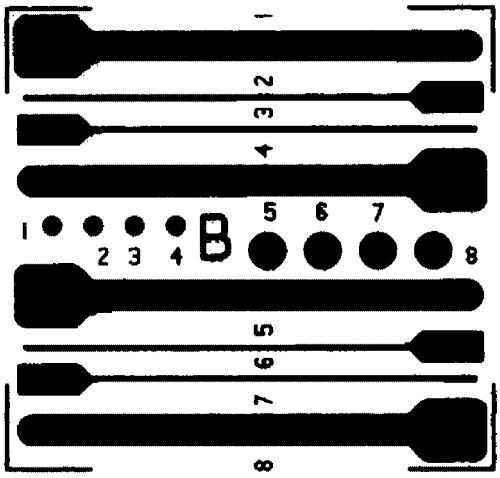
a. Peel strength.

b. Pull-off strength.

For an example of a test specimen B, see Figure 4.

Capability for all types of PCBs

- Conductor adhesion or plating adhesion.
- Peel strength of foil lamination.
- Pull-off strength of surface mount pads.
- Surface solderability.



NOTE This is a surface pattern only and all holes are non-plated-through.

Figure 4: Example of test specimen layout for testing peel strength of conductors and pull-off strength of pads

6.4.3.3 Test specimen C: Electrical test

Internal short circuit.

For an example of a test specimen C, see Figure 5.

Capability for all types of PCBs

Insulation between plated-through holes in daisy chain through all layers and ground plane.

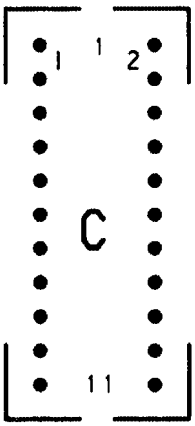


Figure 5: Example of test specimen layout for internal short circuit testing

6.4.3.4 Test specimen D: Electrical test and visual aspect

a. Etching definition.

b. Continuity.

For an example of a test specimen D, see Figure 6.

Capability for all types of PCBs

- Marking.
- Etching definition.
- Continuity between plated-through holes in daisy chain through all layers.
- Visual aspect.

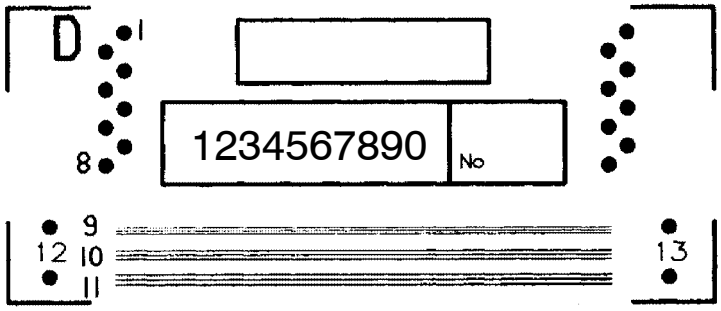


Figure 6: Example of test specimen layout for etching definition evaluation and continuity testing

6.4.3.5 Test specimen E: Electrical test

a. Interconnection resistance.

b. Current overload: short or long duration.

For an example of a test specimen E, see Figure 7.

Capability for all types of PCBs

- Interconnection resistance between plated-through holes in daisy chain through all layers before and after thermal cycling and thermal stress.
- Current overload between plated-through holes in daisy chain through all layers for short time and long time.

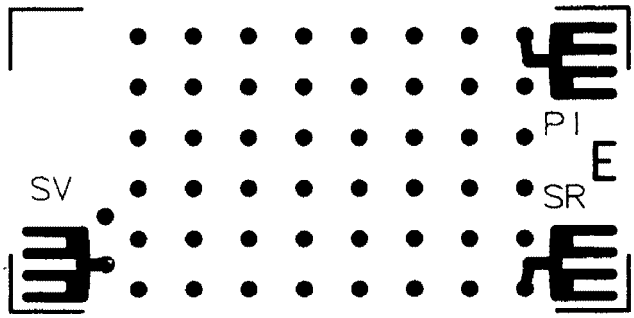


Figure 7: Example of test specimen layout for interconnection resistance and current overload testing

6.4.3.6 Test specimen F: Metal-plating test

Microsectioning.

For an example of a test specimen F, see Figure 8.

Capability for all types of PCBs

- Microsectioning to evaluate and determinate metal plating thickness.
- Microsectioning after thermal cycling, thermal stress and damp heat (optional).

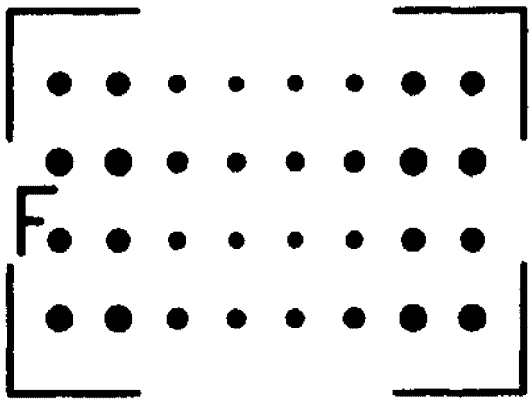


Figure 8: Example of test specimen layout for microsectioning and metal plating evaluation

6.4.3.7 Test specimen G: Metal-plating/coating test

a. Plating adhesion.

b. Analysis of SnPb composition.

For an example of a test specimen G, see Figure 9.

Capability for all types of PCBs

- Plating adhesion on Cu for non-fused SnPb finishes.
- Analysis of SnPb composition after reflow.

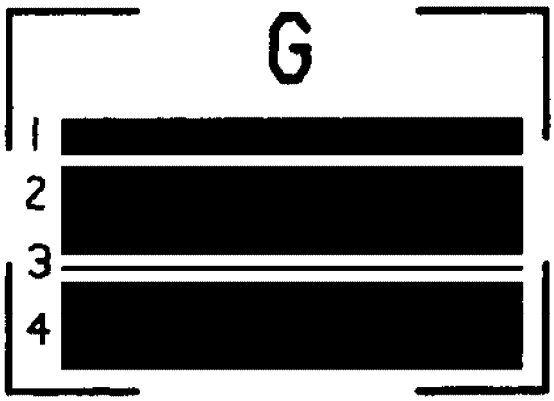


Figure 9: Example of test specimen layout for plating adhesion testing and analysis of SnPb coating composition after reflow

6.4.3.8 Test specimen H: Electrical test

a. Interlayer insulation resistance.

b. Dielectric withstanding voltage.

For an example of a test specimen H, see Figure 10.

Capability for all types of PCBs

- Interlayer insulation resistance and dielectric withstanding voltage before and after thermal cycling and damp heat (optional).
- Interlayer insulation resistance and withstanding voltage measured between plated-through holes and a central ground plane.

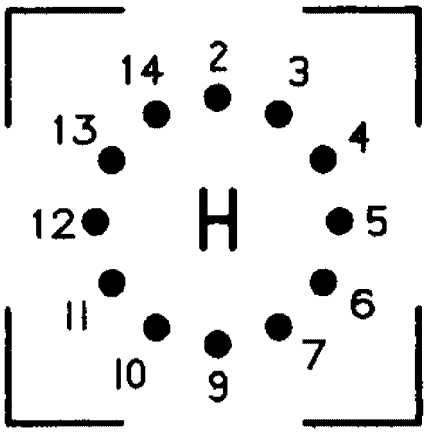


Figure 10: Example of test specimen layout for interlayer insulation resistance and dielectric withstanding voltage testing

6.4.3.9 Test specimen J: Solderability test

a. Solder wettability.

b. Rework simulation.

For an example of a test specimen J, see Figure 11.

Capability for all types of PCBs

- Wettability of solder pads and plated-through holes.
- Evaluation of plated-through hole resistance to rework or repair.

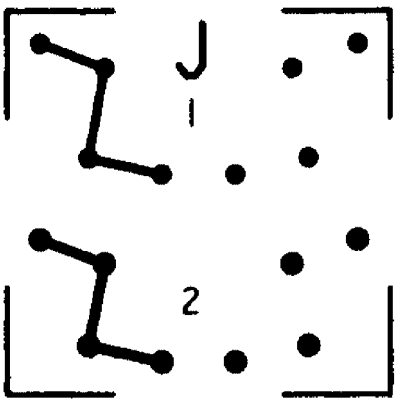


Figure 11: Example of test specimen layout for solder wettability and rework simulation testing

6.4.3.10 Test specimen K: Physical test

a. Water absorption (optional).

b. Outgassing.

For an example of a test specimen K, see Figure 12.

Capability for all types of PCBs

- If the PCB base material is hygroscopic special care shall be taken before assembly.
- Outgassing shall be performed on base laminate material according to ECSS-Q-70-02.

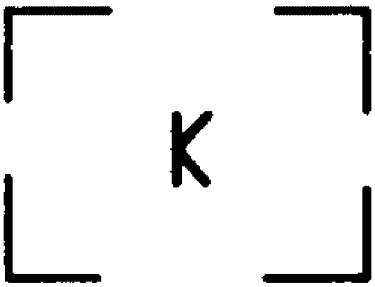


Figure 12: Example of test specimen layout for water absorption and outgassing testing

6.4.3.11 Test specimen L: Capability

a. Minimum conductor width.

b. Minimum spacing.

c. Minimum holes diameter.

d. Other important parameters.

For an example of a test specimen L, see Figure 13.

Capability for all types of PCBs

The capability specimen shall be designed to evaluate the capability of the supplier.

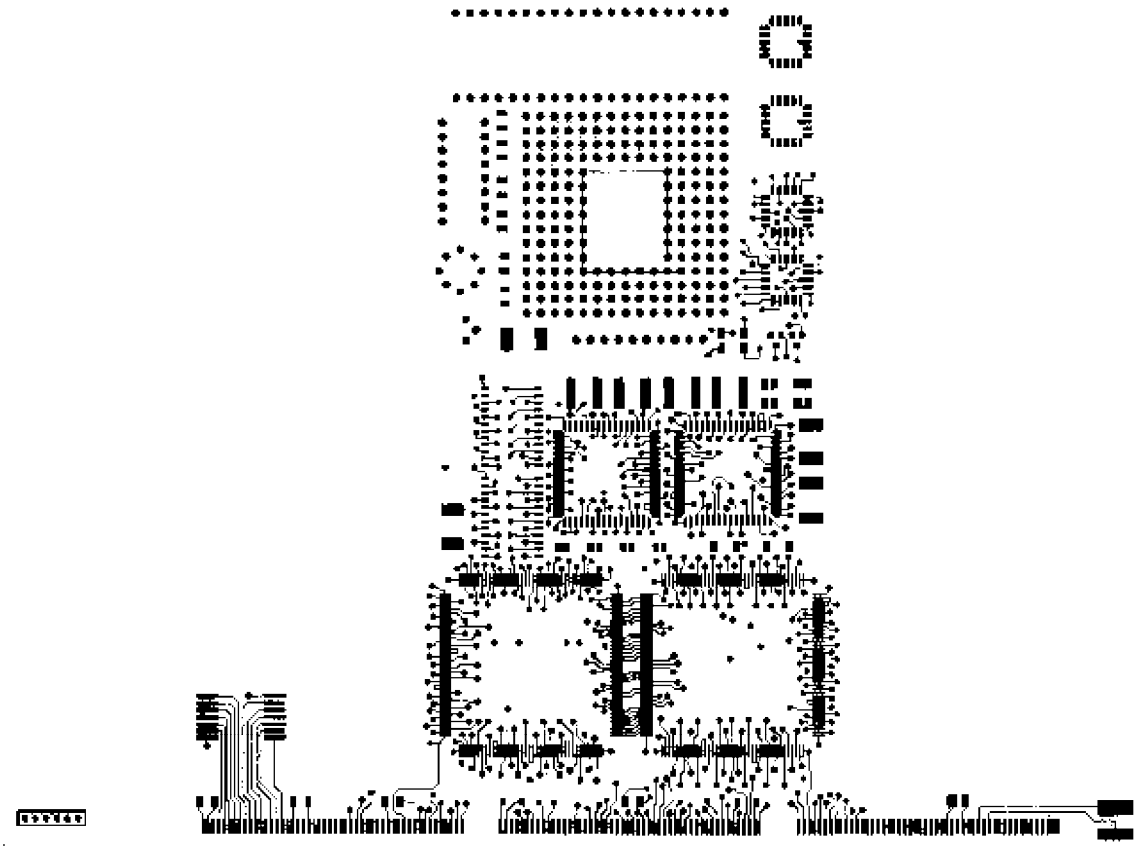


Figure 13: Example of test specimen layout for evaluation of capability limits

6.4.3.12 Test specimen M: CAD/CAM criteria
(on request only)

a. The coupon is divided up into 3 zones with identical surfaces.

b. Various pads in each zones (circular, oblong, square, rectangular).

c. Thermal shunt for internal layer.

For an example of a test specimen M, see Figure 14.

Capability for all types of PCBs

Specimen shall be designed to evaluate the CAD/CAM capability of the supplier.

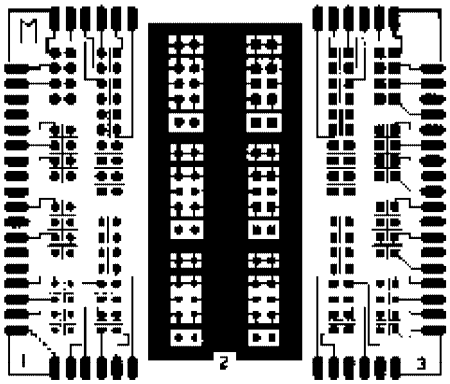


Figure 14: Example of test specimen layout for evaluation of CAD/CAM capability

6.4.3.13 Test specimen X: Resistance to bending cycles

Resistance to bending.

For an example of a test specimen X, see Figure 15.

Capability for all types of PCBs

- Evaluation of continuity of conductors in flexible part.
- Evaluation of adhesion of conductors and insulating material.

Figure 15: Example of test specimen layout for testing resistance to bending cycles

6.4.3.14 Test specimen Y: Electrical test
(on request)

Impedance.

For an example of a test specimen Y, see Figure 16.

Capability for all types of PCBs

Evaluation of controlled impedance capability.

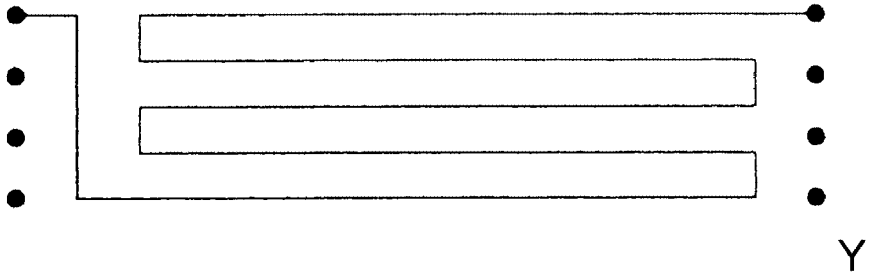


Figure 16: Example of test specimen layout for controlled impedance testing

6.4.3.15 Test specimen W: Electrical test for high frequency circuits
(on request)

a. Dielectric constant.

b. Loss tangent.

Capability for all types of PCBs

Resonator for dielectric constant and loss tangent measurements (to be defined between supplier and customer). The resonator will depend on the dielectric parameters of the material.

6.5 Qualification programme

6.5.1 General

- The qualification programme of PCBs for space applications shall be performed on the six PCB qualification test boards.
- One additional PCB qualification test board shall be made for reference.
- The qualification test boards shall be manufactured according to ECSS-Q-70-11.
- The qualification programme shall be performed by the customer, one or more independent test houses or the PCB supplier. Each test house shall have customer approval prior to commencement of the programme. The programme shall be monitored by the customer at various stages during testing. A comprehensive test report shall be established for review together with all microsections.
- In the case of a qualification extension due to changes in technology the extension qualification programme and qualification test boards shall be negotiated between the customer and supplier.
- If the PCBs are used for manned space programmes the customer shall assure the PCB base material is tested for flammability according to ECSS-Q-70-21 as well as offgassing (toxicity) and odour according to ECSS-Q-70-29. This is the responsibility of the customer.

6.5.2 Nonconformance criteria

- PCB process nonconformances shall be subjected to the dispositions as defined according to quality assurance requirements in ECSS-Q-20-09.
- The nonconformance criteria for a specific test is detailed in the relevant test clause and the minimum requirement for the specific type of PCB is detailed in the relevant table in clause 17.
- Major and minor nonconformances.
  1. Any major nonconformance (**M**) can result in the failure of qualification. This is dispositioned at a nonconformance review board (NRB) established by the customer and the PCB supplier.
  2. Minor nonconformances (**m)** shall be reported and submitted with the qualification report and are considered in the customer's judgement of qualification approval. The supplier shall initiate an internal NRB to determine the causes and consequences.
  3. If a criterion is marked **m**/**M**, the supplier shall agree with the customer what is to be regarded as a minor or a major nonconformance.

7

Test and inspections

7.1 Test condition

Unless otherwise specified, all tests shall be carried out under normal atmospheric conditions (specification IEC 60326-2 am 1 (1992-06) test 18 a).

- Room temperature: (22 ± 3) °C
- Relative humidity: (55 ± 10) %
- Atmospheric pressure

Before testing is started, the PCBs shall be subjected for 48 h to ambient conditions.

During a sequence of measurements, the atmospheric conditions in the test area shall not undergo significant or rapid changes. These conditions shall be noted in the test reports. In case of dispute, the measurements shall be taken under reference atmospheric conditions.

The PCBs to be tested shall not be covered with a protective varnish.

During the testing period, the following precautions shall be taken:

- Keep the boards flat against a plane surface.
- Boards used for electrical tests shall be protected from any contamination and shall be held by their edges during the tests.
- Before environmental exposure, soldering operation, electrical and mechanical testing, the boards shall be cleaned according to ECSS-Q-70-08.

7.2 Test descriptions

The following clauses give the description of the tests for the PCB specimens according to Figure 1 and Table 1. The accept/reject criteria are given with indication of major (**M**) or minor (**m**) nonconformances (see 6.5.2).

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8

Group 1 — Initial test

8.1 Subgroup 1.0 - Visual inspection and non-destructive test

8.1.1 Verification of marking

a. Procedure

Each board shall be inspected with the naked eye for correct marking. The marking shall be legible and resistant to test stresses.

b. Nonconformance criteria

Identification impossible	**M**
Marking not conforming to customer specification	**M**
Defects not affecting identifications	**m**

8.1.2 Visual aspects

a. Procedure

Each board shall be inspected by magnification $\leq \times 10$ with suitable lighting conditions to verify that construction and workmanship meet the requirements. In case of any irregularity, the area shall be examined under $\times 20$ - $\times 40$ magnification.

b. Nonconformance criteria

1. **General cleanliness and contamination**

Contamination visible to the naked eye and not removable by cleaning according to ECSS-Q-70-08	**M**
Contamination visible to the naked eye but removable by cleaning according to ECSS-Q-70-08	**m**

2. **Substrate**

Not in conformity with suppliers trademark and required quality	**M**
Scratches cutting glass fibre or leaving marks in the dielectric affecting reliability	**M**
Scratches not affecting reliability	**m**

Dents, crazing and haloing – visible to the naked eye – not visible to the naked eye	 **M** **m**
Non-homogeneity regarding colouring and opacity	**m/M**
Discoloured copper oxide layer on internal layer is acceptable	
Inclusion of foreign matter, blistering or air bubbles – visible to the naked eye – not visible to the naked eye	 **M** **m**
Delamination	**M**
Measling – generalized – localized reducing insulation distance in the outer layer out of tolerance – localized not reducing insulation distance in the same layer out of tolerance	 **M** **M** **m**
Fungus growth	**M**
Delamination of cover lay (flexible PCB)	**m/M**

3. **Non-plated-through holes**

Holes plated unintentionally	**m/M**
Incompletely drilled holes, missing or additional holes	**m/M**

4. **Routing**

Incomplete routing of board, so that dimensional or mechanical requirements are not met	**M**
Random cutting defects acceptable within the dimensional requirements	**m**

5. **Surface metallization**

Conductors or pads not conforming to customer's layout	**M**
Terminal pads or conductors completely or partially missing, cut, forming a short circuit	**M**
Lifting of conductive pattern from substrate	**M**
Scratches exposing copper plating	**M**
Copper or nickel visible on top surface plated areas	**M**
Large number of superficial scratches not attributed to a manufacturing process evidencing bad workmanship	**M**
Dewetting of solder pads on fused tin lead finish	**M**
Granular aspect of solder pads on fused tin lead finish	**m/M**
Corrosion of copper	**M**
Migration of copper through gold	**M**

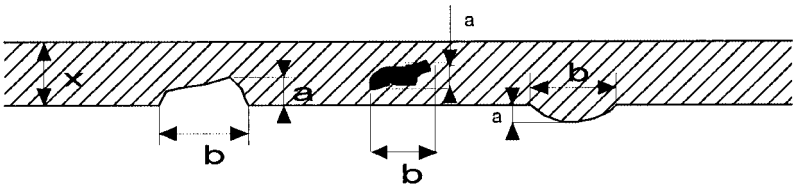
6. **Plated-through holes**

Incompletely drilled, additional or missing holes	**M**
Missing metallization	**M**
Component holes ≥ 0,6 mm filled or partially filled with solder resulting in out of tolerance diameter	**m/M**

7. **Random defects of conductors and terminal pads**

Intermittent and irregular defects which affect metallization, e.g. edge roughness (peak or valley), pits, pin holes, voids, protrusions or indentations.

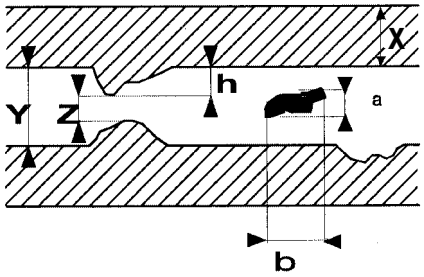
Protrusion or indentations of metallization on conductor edge or voids in conductor as shown in Figures 17, 18 and 19.



x: nominal conductor width

Figure 17: Random defects of conductors and terminal pads

a ≤ 20 % of x and conductor width > minimum requirement	**m**
a > 20 % of x or conductor width < minimum requirement	**M**
b ≤ x	**m**
b > x	**M**



y: nominal spacing between conductors

Figure 18: Random defects between two conductors

Opposite peaks: if z < 80 % of y	**M**
Isolated peaks or valleys: h > 20 % of x and z < minimum requirement	**M**
Conducting island: a + h > 20 % of y and the isolation spacing < minimum spacing requirement	**M**
a > 20 % of y or y – a < minimum requirement	**M**
b > y	**M**
Cover lay (flexible PCBs) covering part of solder pad	**M**

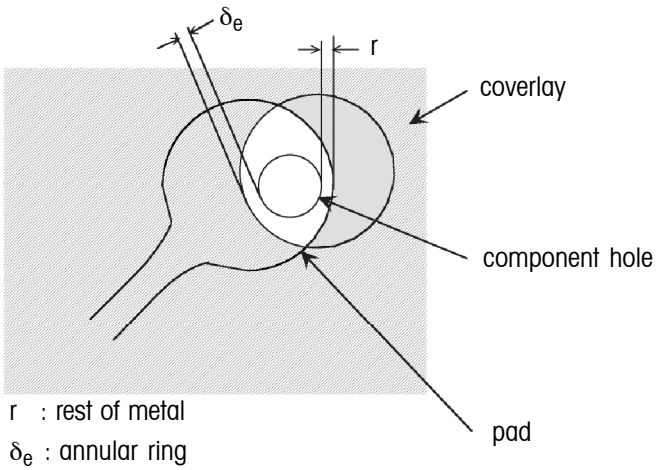


Figure 19: Misalignment of coverlay

8.1.3 External dimensions

a. Procedure

Each board shall be measured by means of suitable standard measuring equipment to verify that the physical dimensions, including board thickness and external dimensions meet the customer's specifications.

b. Nonconformance criteria

1. Thickness of base laminate
(average of 4 measurements on the board)

If out of tolerance	**M**

2. Length and width of board
(average of 2 measurements on the board)

If out of tolerance	**M**

8.1.4 Warp

a. Procedure

The PCBs shall be placed unrestrained on a plane horizontal surface with the convex side upward. The warp shall be expressed in percentage terms.

- Measure maximum bow between the plane horizontal surface and the PCB as defined in Figure 20.
- Measure the length of the PCB.
- Calculate the warp percentage:

$$\text{Warp} \quad \% = \frac{\text{Max. blow in mm}}{\text{Length of the PCB in mm}} \times 100$$

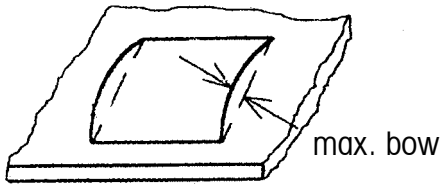


Figure 20: Warp

b. Nonconformance criteria

If more than maximum bow	**M**

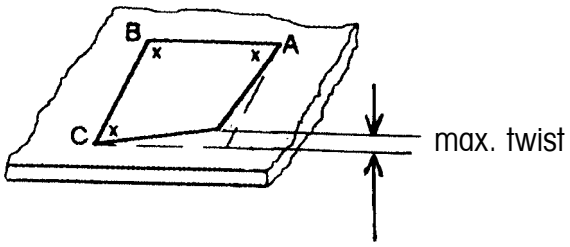
8.1.5 Twist

a. Procedure

The PCB shall be placed on a plane horizontal surface so that it rests on three corners. The height of the remaining corner from the surface shall then be measured (expressed in percentage terms).

- Measure the distance between the plane horizontal surface and the fourth corner of the PCB, as defined in Figure 21.
- Measure the length of the diagonal.
- Calculate the twist percentage:

$$\text{Twist} \quad \% = \frac{\text{Max. twist in mm}}{\text{Length of the diagonal in mm}} \times 100$$



A, B and C are touching base

Figure 21: Twist

b. Nonconformance criteria

If more than maximum twist	**M**

8.2 Subgroup 1.1 — Specific dimensional check

a. The points to be measured on test coupons and circuit shall be decided between suppliers and customers and shall include for example:

- minimum and maximum plated-through holes diameter and soldering pads diameter;
- minimum and maximum conductor width;
- minimum and maximum distance between conductors.

b. The measurements shall be presented in tabular form for better readability.

Plated-through holes					
Measuring point	Test or coupon	Ø pad		Ø hole	
		Measured	Deviation	Measured	Deviation

Conductor's widths			
Measuring point	Test or coupon	Measured dimension	Deviation

Spacing between conductors			
Measuring point	Test or coupon	Measured dimension	Deviation

c. Procedure

Measurements of dimensional parameters relating to metal plating (e.g. width of conductors, spacing, minimum annular ring metal) shall be taken at the copper/board base interface or for high frequency circuits as required by the customer (see subclause 9.3 Figure 23). Hole diameters may be measured with measuring gauges or a measuring microscope.

d. Nonconformance criteria

All dimensions (e.g. diameter of holes, width of conductors and diameter of terminal pads) which do not conform to the circuit definition document and acceptable tolerance limits	**M**
For non-soldering holes: diameter out of tolerance	**m**

8.3 Subgroup 1.2 — Electrical measurements

8.3.1 Intralayer insulation resistance on specimen A

According to tests 6a and 6b of IEC 60326-2 am 1 (1992-06).

a. Procedure

A direct voltage of (500 ± 50) V shall be applied between the two closest conductors which are not electrically connected. The insulation resistance (R) is measured 1 min after the voltage has been applied.

b. Nonconformance criteria

If R is less than minimum requirement	**M**

8.3.2 Interlayer insulation resistance on specimen H

According to tests 6c of IEC 60326-2 am 1 (1992-06).

a. Procedure

Carry out the test as before, the voltage being applied between two ground planes (or between one ground plane and one conductor) that are superimposed.

b. Nonconformance criteria

If R is less than minimum requirement	**M**

8.3.3 Dielectric withstanding voltage intralayer on specimen A and interlayer on specimen H

According to tests 7a and 7b of IEC 60326-2 am 1 (1992-06).

a. Procedure

The test voltage shall be applied between two superimposed conductors (i.e. between layers), or between two adjoining (but not electrically connected) conductors within the same layer. The AC voltage at 50 Hz is gradually applied progressing from 200 V r.m.s. per second up to 1 500 V r.m.s. per mm of spacing between two conductors. This voltage shall be kept steady for one minute, with the current limited to 100 μA.

Final measurements: aspect and continuity.

b. Nonconformance criteria

Evidence of breakdown, flashover or sparking	**M**

8.3.4 Continuity on specimen D

According to test 3a of IEC 60326-2 am 1 (1992-06).

Conductor continuity is tested by measuring the interconnection resistance on specimen D.

a. Procedure

The measurement shall be taken using a method ensuring an error no greater than 5 % (four wires method).

The current shall be limited to 0,1 A.

The measuring voltage shall not exceed 5 V.

The post-test measurements taken on each sample shall be compared with pre-test measurements.

b. Nonconformance criteria

Discontinuity	**M**
Dispersion greater than ±10 % with respect to the mean of values measured on the specimens	**m/M**

8.3.5 Interconnection resistance on specimen E

According to test 3b of IEC 60326-2 am 1 (1992-06).

a. Procedure

Same test conditions as for continuity testing.

b. Nonconformance criteria

Discontinuity	**M**
Dispersion greater than ±10 % with respect to the mean of values measured on the specimen	**M**

8.3.6 Impedance test on specimen Y

According to test 9a of IEC 60326-2 am 1 (1992-06).

The measuring method shall be specified by the customer.

8.3.7 Dielectric constant and loss tangent for high frequency materials on specimen W

The measuring method shall be specified by the customer.

- Annular ring.
- Closed cavity or other method.

9

Group 2 — Miscellaneous tests

9.1 Subgroup 2.1 — Solderability test — Wettability on specimen J

According to test 14a of IEC 60326-2 am 1 (1992-06) and IEC 60068-2-20 am 2 (1987-01), test TC.

a. Procedure

- Non-activated rosin-based flux as specified in ECSS-Q-70-08.
- Solder
  Tin lead 60/40 or 63/37 as specified in ECSS-Q-70-08.
- Test machine
  Rotary dip tester or similar equipment.

The specimens are fluxed by immersion.

Surplus flux is removed by keeping the specimens upright for 5 min.

The specimen is arranged on the soldering machine and brought into contact with the surface of the solder bath that is kept at the temperature of (235 ± 5) °C during:

- 3 s (wetting time),
- 10 s (dewetting time).

b. Inspection

A visual inspection is made with a ×10 magnification.

A microsection can also be performed and a visual inspection made at a magnification greater than ×100.

c. Nonconformance criteria

Poor wettability of solder pads and plated-through holes: see Figure 22	**M**
Microsectioning Broken metallization	 **M**

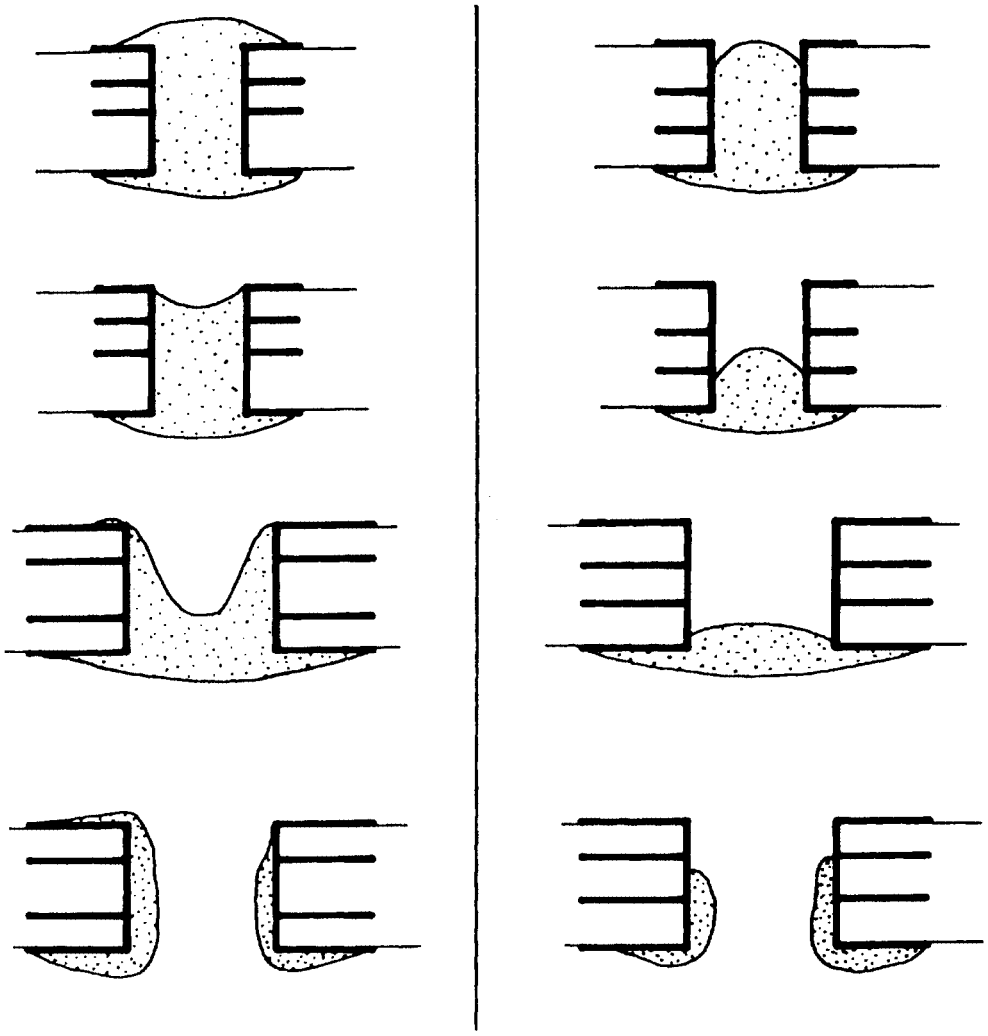


Figure 22: Wettability of terminal pads and plated-through holes

9.2 Subgroup 2.2 — Mechanical tests

9.2.1 Peel strength on specimen B

According to test 10a of IEC 60326-2 am 2 (1992-06).

a. Procedure

The conductor selected is peeled back at one end for a length of about 10 mm.

The detached end of the conductor is firmly gripped over its whole width and traction is then applied in a direction perpendicular to the plane of the PCB until the copper starts to peel away.

The rate of traction is kept constant at 50 mm/min. The traction direction is kept perpendicular to the plane of the PCB. Machine inertia shall have no effect on the measurement. The conductor width to be taken into account shall be the actual width where the conductor is stuck to the insulation.

b. Nonconformance criteria

Peel strength

If less than minimum requirement	**M**

9.2.2 Pull-off strength on specimen B

According to test 11a of IEC 60326-2 am 1 (1992-06).

a. Procedure

- Temperature of iron: (270 ± 10) °C.
- Solder: Tin-lead 60/40 or 63/37 alloy with non-corrosive resin core as specified in ECSS-Q-70-08.

After application of the soldering flux specified in IEC 60068-2-20 am 2 (1987-01), test TC, the pads shall be tinned for (4 ± 1) sec.

A tinned copper wire with a diameter 0,3 mm less than the hole diameter and of 150 mm approx. lengths shall be used.

Soldering shall be between 2 s and 3 s.

After another 5 min ambient reconditioning the soldering operations shall be repeated (second soldering).

- Ambient reconditioning:

  The ambient reconditioning time before final measurement shall be more than 10 min.

- Final measurement:

  Force is applied using a traction machine pulling on the wire. This force increases with a constant rate of between 5 N/s and 50 N/s until the terminal pad separates from the board base material (chosen value 10 N/s).

b. Nonconformance criteria

Pull-out strength for terminal pads.

If less than minimum requirement	**M**

9.2.3 Flexural fatigue on specimen X (for double sided flexible PCB)

According to test 21a of IEC 60326-2-am 1 (1992-06).

a. Procedure

Equipment similar to that described in IEC 60249-1-am 4 (1993-05) sub-clause 3.12-2 and Figure 13.

Short insulated wires are connected to the ends of the conductive patterns (front and backsides in series). The test specimen is mounted on the device such that the interior diameter of the loop is (9,6 ± 0,4) mm.

The alternating movement shall be such that the loop moves at least 25 mm and that the test specimen is not curved at either end.

The pace of the alternating movement shall not exceed ten cycles per minute.

The test consists of maintaining the alternative movement until an electrical discontinuity appears or until the 500 cycles required is completed without a defect.

b. Nonconformance criteria

Discontinuity appearing before 250 cycles	**M**
Discontinuity appearing between 250 cycles and 500 cycles	**m**
Lifting of conductors from insulation coating	**m/M**
Lifting of conductors from board base material	**m/M**
Lifting of insulation coating from board base material	**m/M**

9.2.4 Bending test for rigid-flex

According to MIL-P-50884C Para. 3.6.5 and 4.8.4.5.

a. Procedure

25 cycle folding test as described in subclause 4.8.4.5.

b. Nonconformance criteria

There shall be no electrical defect or degradations

Any degradation of continuity	**M**

9.3 Subgroup 2.3 — Coatings tests

9.3.1 Coating adhesion of non-fused SnPb finishes on specimen G

According to test 13a of IEC 60326-2 am1 (1992-06).

a. Procedure

This test shall be performed on SnPb finished boards before reflow of test board.

After cleaning, an adhesive tape, at least 50 mm long, is applied to the test surface and pressed down to eliminate all air bubbles.

After 10 s, the tape is quickly pulled off perpendicular to the coating surface. The surface area to be tested shall be 1 cm^2 of conductor (example of tape to be used: TESA 4104 width 19 mm).

b. Nonconformance criteria

If part of SnPb coating is sticking to tape or test surface shows scaling	**M**

9.3.2 Analysis of SnPb coating on specimen G

a. Procedure

Proposed method for SnPb: the tin-lead alloy shall be chemically dissolved. The relative quantities of tin and lead shall be determined by atomic absorption spectrometry.

Any other method resulting in the same degree of precision may be used.

b. Nonconformance criteria

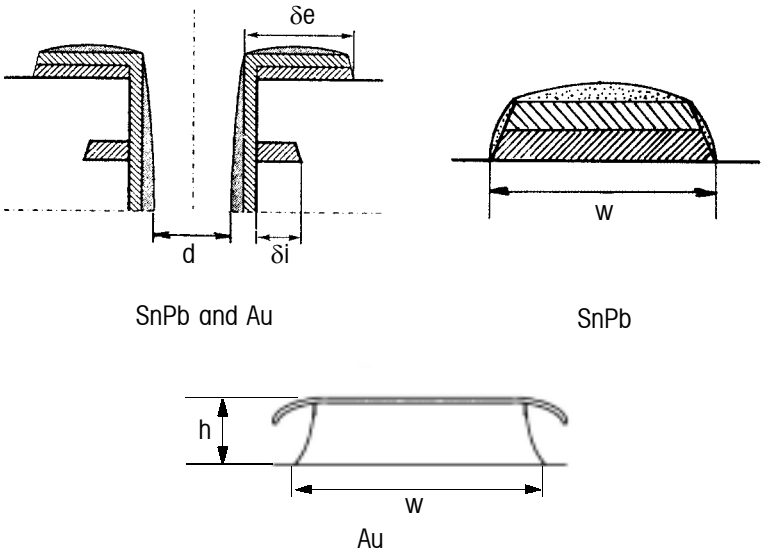
If out of tolerance	**M**

9.3.3 Microsectioning on specimen F

9.3.3.1 General

Microsection with typical defects in PTH is shown in annex D.

According to tests 1c and 15b of IEC 60326-2-am1 (1992-06), for high frequency conductors the customer shall specify at which height of the conductor the width shall be measured (see Figure 23).



w width of conductor
δe minimum annular ring on external layer
δi minimum annular ring on internal layer
d diameter of plated-through hole
h height of conductor

Figure 23: Dimensional parameters to be measured

9.3.3.2 Thickness of metal-plating

a. Procedure

Test carried out on a microsection and observations made with magnification greater than or equal to ×250.

b. Nonconformance criteria

1. **Thickness of copper plating on external layers**

(a) basic copper

Value not conforming to that specified	**M**

(b) basic copper plus electrolytic copper on non-soldering areas

If thickness is less than specified	**M**

(c) basic copper plus electrolytic copper soldering pads (see Figure 24 number 2)

If thickness < 40 μm	**M**

2. **Thickness of copper in plated-through holes (component holes)**

   Average thickness based on 3 measurements taken on the hole walls (see Figure 24 number 1)

If less than minimum requirement	**M**

3. **Thickness of copper layer on internal layers**

If not conforming to specified thickness	**M**

4. **Thickness of copper in plated-through holes (via, buried via and blind via)**

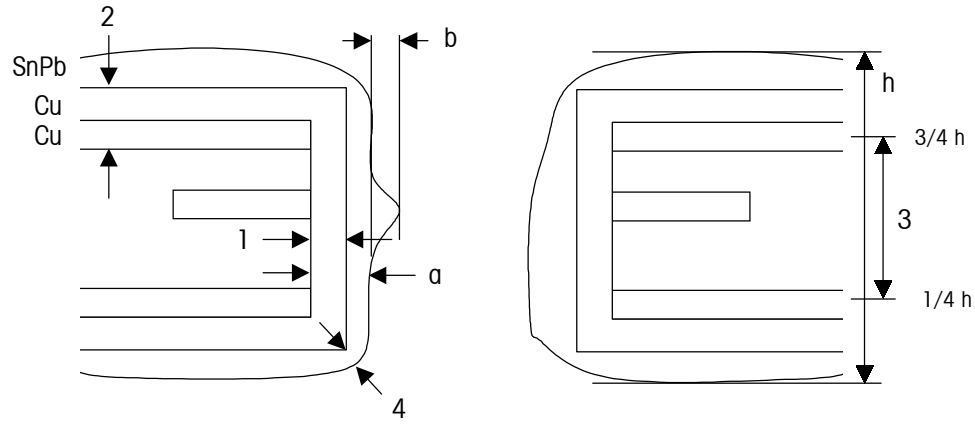
If less than minimum requirement	**M**

5. **Thickness of tin-lead alloy on surface (measured along the conductor longitudinal axis)**

If thickness > 5 µm and < 8 µm	**m**
If thickness < 5 µm	**M**

6. **Thickness of tin-lead alloy in holes**

If thickness < 8 µm in highest part of half of the hole wall height (see Figure 24 number 3)	**M**
If thickness between 1 µm and 2 µm over angle of hole corner (see Figure 24 number 4)	**m**
If thickness < 1 µm in angles (see Figure 24 number 4)	**M**



Key

1 = Cu in PTH

2 = Cu at surface pattern

3 = SnPb in hole

4 = Sn/Pb in angle area

internal bulging b < a

Figure 24: Microsection of a PTH

7. **Thickness of electrolytic Au or Au/Ni on surface and in holes (measured along the conductor longitudinal axis)**

Au for manual soldering on nickel	
- if thickness < 1 μm	**M**
- if thickness > 7 μm	**M**
Au for manual soldering on copper	
- if thickness < 3 μm	**M**
- if thickness > 7 μm	**M**
Au for high frequency circuits or other assembly methods - as specified by customer	
- if out of specified tolerance	**M**
Ni	
- if thickness < 2 μm	**M**
- if thickness > 10 μm	**M**

8. **Distance between SnPb and Au overlap and the termination pad designated for soldering**

If distance < 200 μm	**M**

9. **Etch undercut for fused SnPb (see Figure 25) and Au with or without Ni finishes (see Figure 26)**

External and internal layers	
- if undercut (u) > total copper thickness (h)	**M**
- if undercut (d) > 30 μm for Au with or without Ni finish	**M**

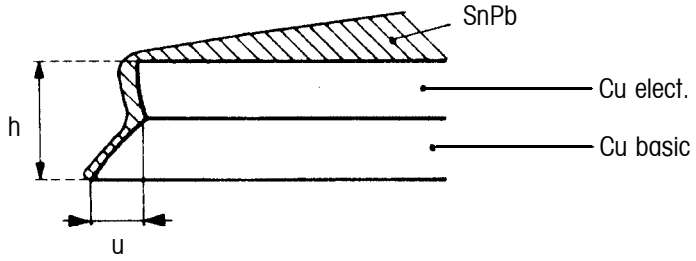


Figure 25: Undercut for PCBs with fused SnPb finish

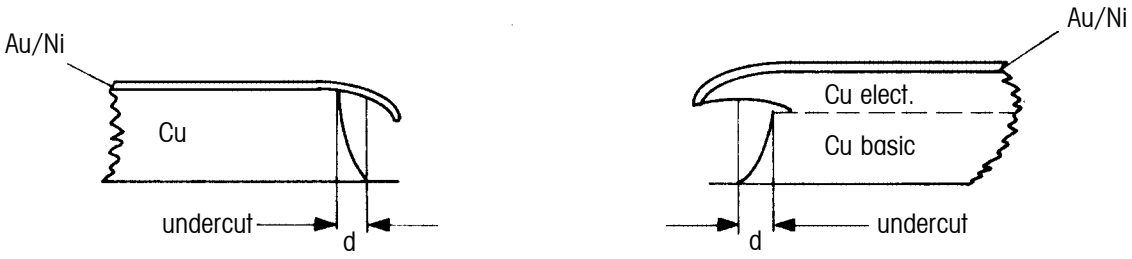


Figure 26: Undercut for PCBs with Au/Ni or Au finish

10. **Etch overhang for Au with or without Ni finish (see Figure 27)**

External layers if overhang (D) > 2 × thickness of total copper and Au/Ni or Au	**M**

NOTE For high frequency application overhang is normally undesirable and may be removed mechanically.

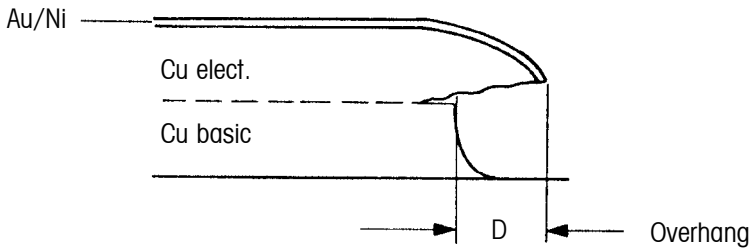


Figure 27: Overhang for PCBs with Au/Ni or Au finish

9.3.3.3 Aspect of plated-through holes

a. Procedure

Sections of plated-through holes are observed with magnification greater than or equal to ×100.

b. Nonconformance criteria

Layer misregistration compared to the minimum annular ring on pads.

1. External layer (see Figure 23)

If δe less than minimum requirement	**M**

2. Internal layer (see Figure 23)

If δi less than minimum requirement	**M**
If minimum insulation between layers less than minimum requirement	**M**

3. Irregular drilling (see Figure 28)

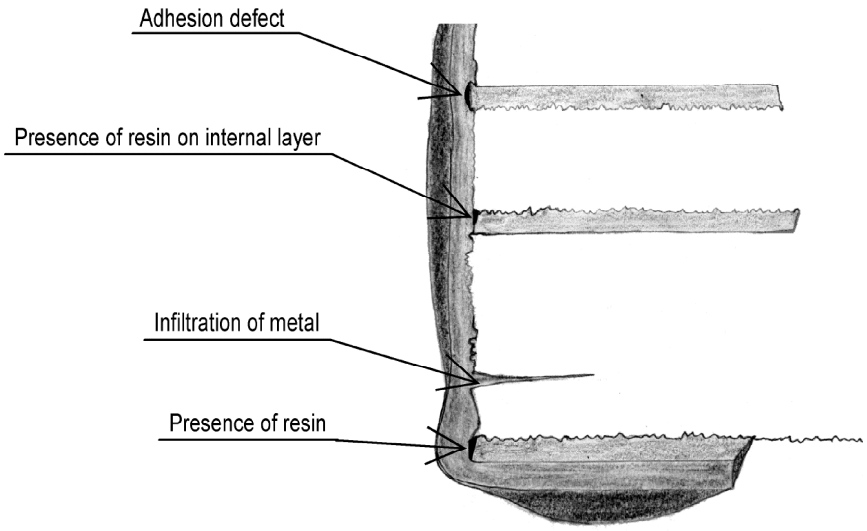
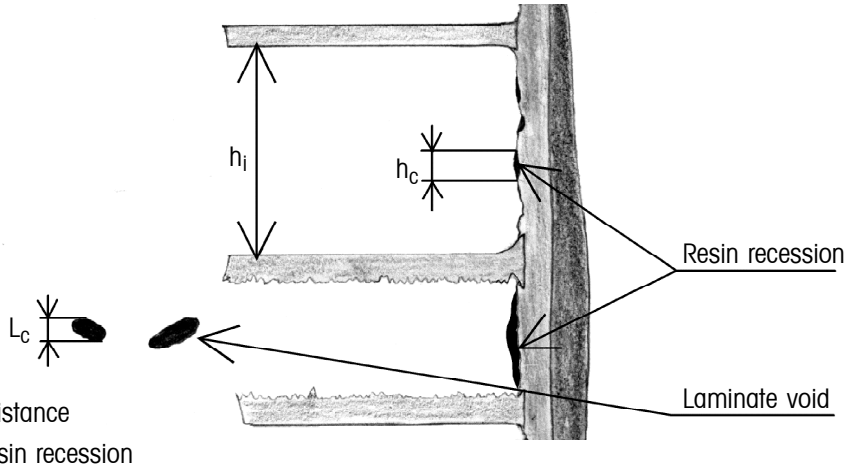


Figure 28: Microsection in PTH: Possible defects

Infiltration of metal into base laminate – between 40 µm and 80 µm – greater than 80 µm	 **m** **M**
Presence of adhesive on basic copper not leading to rupture during fusing process or thermal shock	**m**
Adhesion defects between metal-plating and basic copper	**M**
Adhesion defects between metal-plating and inner layers	**M**
Resin smear on internal conductor/plated copper interface greater than 15 % of conductor thickness	**M**
Void in resin greater than 50 % of basic copper thickness	**M**

4. Voids in PCB base laminate substrate and resin recession in holes (see Figure 29)



h_i = insulation distance
h_c = height of resin recession
L_c = size of the void

Figure 29: Microsection of PTH: Possible defect

Voids in the PCB base laminate substrate and around the metal-plating (resin recession) - if void Lc > 80 µm At edge of metal-plating - if sum of resin recession h_c > 20 % sum h_i	 **M** **M**
Resin recession in hole before or after test - if 10 % of height of hole < resin recession < 20 % of height of hole - if resin recession > 20 % of height of hole	 **m** **M**

5. Copper plating inside buried, blind, via and component holes

Void of copper plating in holes	**M**

6. Resin inside buried vias (see Figure 30)

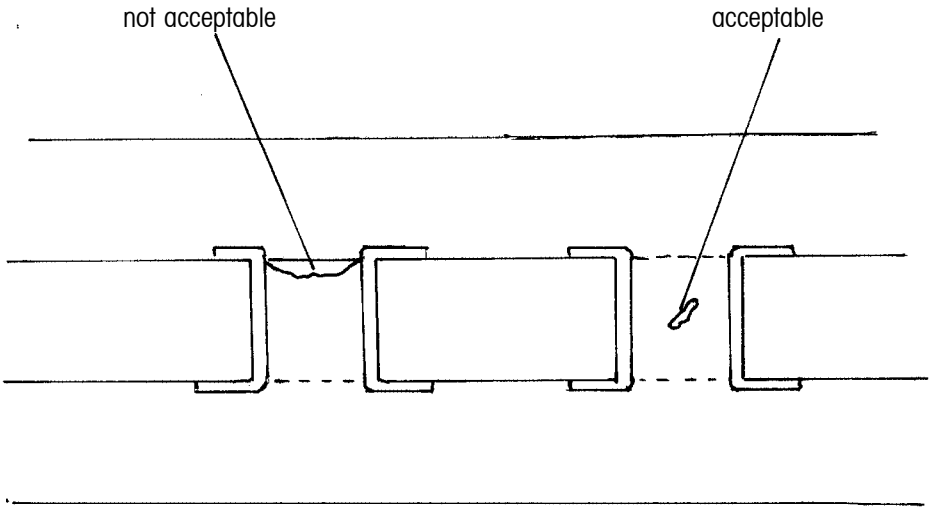


Figure 30: Voids in resin inside buried vias

9.4 Subgroup 2.4 — Electrical tests

9.4.1 Current overload on specimen E

According to test 5 of IEC 60326-2-am 1 (1992-06).

9.4.1.1 Short-time overload

a. Procedure

The test shall be carried out on a pattern including holes connected (50 holes minimum) in series by conductors.

Two connecting wires are soldered to both ends of the circuit being tested.

A measurement is taken of the interconnection resistance between the ends.

Voltage is applied between ends in such a way that current flow into the circuit is:

- 7 A for 35 µm thick basic copper;
- 14 A for 70 µm thick basic copper.

This voltage is maintained for (4 ± 1) s.

After ambient reconditioning for 2 h, circuit continuity is checked by measuring the interconnection resistance.

b. Nonconformance criteria

Electrical discontinuity	**M**
Blistering visible to the naked eye	**M**
Variation in interconnection resistance increased by more than +10 %	**M**

9.4.1.2 Long-time overload

a. Procedure

Same initial conditions as previously with application of a voltage to the circuit terminals such that the current varies by successive steps:

I_0 = 2 A for 3 min

Then I_1 = 4 A for 3 min and so on with an increment of 2 A every 3 min until destruction (open circuit). However, the test shall be interrupted, if for I = 18 A, circuit discontinuity is not achieved.

b. Nonconformance criteria

If destructive current less than minimum requirement	**M**

9.4.2 Internal short circuit on specimen C

According to test 4a of IEC 60326-2-am 1 (1992-06).

a. Procedure

This test shall be carried out in an insulation area.

Apply a polarized voltage of 100 V DC between the ground plane connected to earth and the plated-through hole passing through the access opening for 1 min (see Figure 31).

Measure the insulation resistance.

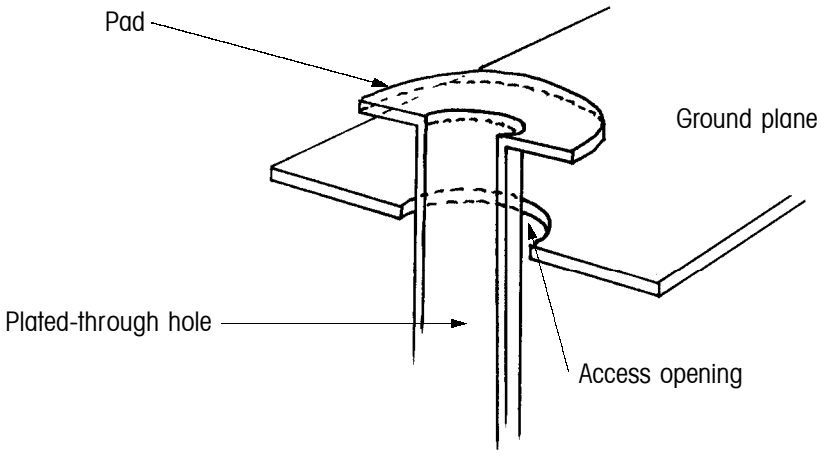


Figure 31: Test for internal short circuit

b. Nonconformance criteria

If insulation resistance is less than minimum requirement	**M**

9.5 Subgroup 2.5 — Physical tests on specimen K

9.5.1 Water absorption (optional)

a. Procedure

The test specimen, completely devoid of copper, is dried in an oven for (24 ± 1) h at 55 °C (+0 °C, -5 °C) then cooled in a container with a siccative until the temperature is (23 ± 1) °C at which stage it is weighed to the nearest milligram.

It is then placed in a de-ionized water bath maintained at (23 ± 0,5) °C.

It shall be placed on the edge, remain completely submerged and not in contact with the edges of the bath.

After (24 ± 1) h, it is withdrawn from the water, dried with a dry fluff-free cloth or filter paper, then weighed to the nearest milligram in the minute following its removal from the water.

b. Nonconformance criteria

Percentage of water absorbed	
- glass fibre-epoxy base laminate > 0,2 %	**M**
- glass fibre-polyimide base laminate > 0,8 %	**M**
- random glass reinforced PTFE resin > 0,2 %	**M**
- ceramic filled woven-glass reinforced PTFE resin > 0,1 %	**M**
- ceramic filled PTFE resin > 0,1 %	**M**
- ceramic filled × linked hydrocarbon/thermoset polymer > 0,1 %	**M**
- quartz filled polyimide > 0,8 %	**M**
- polyimide > 0,8 %	**M**

9.5.2 Outgassing

According to ECSS Q-70-02 specification.

a. Procedure

The test is carried out on a test specimen entirely devoid of copper in order to determine the volume of included gas constituents, which threaten to contaminate a space environment.

Determination of outgassing after measurement of the difference in weight of the test specimen before and after the test.

b. Nonconformance criteria

TML or RML > 1 % (see ECSS-Q-70-02A subclause 7.2.3) and CVCM > 0,1 %	**M**

10

Group 3 — Thermal stress and thermal shock (on board)

10.1 General

Solder bath test is to simulate solder wave assembly of PCBs followed by vapour phase solder simulation to simulate solder reflow assembly of PCBs. Rework simulation test simulates hand solder assembly, rework and repair of PCBs.

Omission of any of these tests shall be agreed between customer and supplier.

10.2 Solder bath float method and vapour phase reflow simulation method (on board without specimen F)

10.2.1 Solder bath float

According to test 19c of IEC 60326-2-am 1 (1992-06).

a. Procedure

The thermal shock is applied to one side of the test board by floating it in a solder bath.

After conditioning for 6 h at (140 ± 2) °C, the board shall be floated in a 63/37 solder bath maintained at (287 ± 6) °C.

Duration of test: 10 s.

After ambient reconditioning time of more than 1 h visual inspection is performed: substrate visual aspect.

10.2.2 Vapour phase simulation

According to test 19g of IEC 60326-2-am 1 (1992-06).

a. Procedure

A thermal shock is applied to the whole board of the test board by immersion in the vapour phase of a fluorinated chemical bath.

Depending on the time passed after the first thermal shock, the board shall be conditioned for 1 h to 6 h at (140 ± 2) °C.

The other side of the same test board shall be coated with flux or a solder paste with flux and baked. Thereafter, the test board shall be lowered into the (215 ± 2) °C warm vapour phase.

Duration of test: 10 s

After ambient reconditioning time of more than one hour, final measurements shall be performed:

- substrate visual aspect,
- peel strength on specimen B,
- continuity on specimen D,
- interconnection resistance on specimen E,
- microsectioning on specimen J.

b. Nonconformance criteria

If peel strength is less than minimum requirement	**M**
Delamination	**M**
Localized/generalized measling	**m/M**
Terminal pads beginning lifting-general	**M**
Lifting of terminal pads	**M**
Variation in interconnection resistance > +10 %	**M**
Microsectioning: broken metallization	**M**

10.3 Rework simulation (thermal shock, hand soldering) on specimen F

According to test 19d of IEC 60326-2-am 1 (1992-06).

a. Procedure

A thermal shock is applied to the specimen F by soldering/unsoldering a wire five times.

Copper wires of diameter:

- 0,51 mm for holes of Ø = 0,8 mm (Ø of land = 2 mm),
- 1,02 mm for holes of Ø = 1,6 mm (Ø of land = 4 mm),

and a sufficient length to fit the gripping mechanism of the tensile tester shall be prepared for each hole. The wires shall be inserted in the holes and soldered to the terminal areas. A conventional soldering iron, operating at a tip temperature of (270 ± 10) °C, shall be used.

The wires shall not be clinched on the other side of the PCB. They shall be soldered and then unsoldered and removed from the hole. This cycle shall be repeated five times, using a new wire for each soldering operation. During the soldering/unsoldering cycles, the soldering iron shall be applied to the wire and not to the terminal pads.

After the fifth cycle, the wires shall be soldered into the holes and the PCB shall be left to cool for 30 min minimum.

b. Nonconformance criteria

Microsection the soldered holes to show that copper through-hole plating has not cracked.

If cracked	**M**

NOTE For flexible PCB the high temperature dip test (oil bath) used is according to IEC 60326-2-am 1 (1992-06), test 19a.

11

Group 4 — Thermal cycling (on board)

According to specification IEC 60068-2-14-am 1 (1986-01), test Nb.

a. Procedure

Degree of severity: ΔT shall be 200 °C with the highest temperature not exceeding the glass transition temperature. The lower temperature can be (-70 ± 15) °C.

Number of cycles: 200.

Temperature gradient: approx. 10 °C/min.

Ambient reconditioning time after each extreme temperature time: 15 min.

After ambient reconditioning time greater than 2 h, final measurements are performed:

1. substrate visual aspect,
2. peel strength on specimen B,
3. continuity on specimen D and interconnection resistance on specimen E,
4. intra- and interlayer insulation resistance on specimen A and H,
5. withstanding voltage on specimens A and H,
6. microsectioning on specimen F.

b. Nonconformance criteria

If peel strength is less than minimum requirement	**M**
Variation in resistance > +10 %	**M**
Intralayer insulation resistance < 10^3 MΩ	**M**
Interlayer insulation resistance < 10^4 MΩ	**M**
Evidence of flashover, breakdown, sparking	**M**
Microsectioning: broken metallization	**M**

Technological and functional defects are unacceptable.

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12

Group 5 — Damp heat — Steam ageing (on board)

12.1 Damp heat on board without specimen F

According to specification IEC 60068-2-3 (1969-01), test Ca.

a. Procedure

Degree of stress condition:

— Temperature: (40 ± 2) °C.

— Relative humidity: 93 % (+2 %, -3 %).

— Duration of test: 10 days.

— No operation during test.

After ambient reconditioning to normal atmospheric conditions for a period of at least 1 h and not more than 2 h, final measurements shall be taken:

1. Peel strength on specimen B;
2. Intra- and interlayer insulation resistance on specimens A and H;
3. Withstanding voltage on specimens A and H;
4. Microsectioning (if necessary) on specimen F;
5. Corrosion of circuits for electrolytic Au finish.

b. Nonconformance criteria

If peel strength is less than minimum requirement	**M**
Intralayer insulation resistance < 10^3 MΩ	**M**
Interlayer insulation resistance < 10^4 MΩ	**M**
Evidence of flashover, breakdown, sparking	**M**
Microsectioning (if required): broken metallization	**M**
Evidence of corrosion	**M**

12.2 Steam ageing on specimen F

According to specification IEC 60326-2 am1 (1992-06), test 20a.

This test is intended to give an indication of the effects of storage on the solderability of the PCBs.

a. Procedure

- Flux

  Non-activated rosin-based flux as specified in ECSS-Q-70-08.

- Solder

  Tin-lead 60/40 or 63/37 alloy with non-corrosive resin core as specified in ECSS-Q-70-08.

- Test machine

Steam generator or similar equipment.

The specimens are fluxed by immersion.

Surplus flux is removed by keeping the specimens upright for 5 min.

The specimen shall be exposed in the steam generator machine for approximately 80 min.

1. After closing the generator, it shall be flooded with nitrogen at a flow rate between 250 ml/min and 750 ml/min.
2. Specimen carrier shall rotate at a speed of 5 revolutions per minute to 50 revolutions per minute.
3. Temperature inside machine shall be (100 ± 2) °C and stabilized for (5 ± 1) min. The nitrogen flow shall be switched off.
4. The 90 °C condensed steam rate in the chamber shall be controlled to (5 ± 0,5) l/min.
5. A mixture of pure oxygen 20 % and nitrogen 80 % with a flow rate of (100 ± 10) ml/min is then switched on for (60 ± 5) min.

After removing the specimens from the steam generator machine, they shall be dried and a solderability test shall be performed.

b. Nonconformance criteria

A visual inspection shall be performed with a ×10 magnification.

If the result of the visual inspection is deemed unsatisfactory, a microsection shall be performed. In this case a visual inspection shall be made with a magnification greater than ×100.

Poor wettability of conductors, terminal pads and plated-through holes: see Figure 22 for terminal pads and plated-through holes	**M**
Microsectioning (if necessary): broken metallization	**M**
Evidence of corrosion	**M**

13

Qualification approval

13.1 General customer qualification

The customer shall make the final decision to grant qualification status to the PCB supplier concerned on the basis of examination and acceptance of the fully documented qualification test programme, which shall be compiled by the supplier into a test report/data package and shall contain the results for all tests specified in clauses 7 to 12 .

At this point the processes used for manufacturing space PCBs shall be established and frozen and documented in a process identification document (PID) as mentioned in subclause 5.4. The PID list all the process and control specifications with number, issue number and date for the full manufacturing flow for the qualified PCBs and the limits of approval.

13.2 Validation of qualification

The successfully performed qualification test programme shall be considered valid for a period of two years.

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14

Maintenance of qualification

14.1 General

If problems related to the manufacturing of PCBs for space projects occur, during the qualification period, the supplier shall inform the customer about the problem.

14.2 Maintenance

a. To maintain qualification status, the supplier shall send, two months before the expiry date of the qualification period, a letter to the customer containing the following information:

   1. List of changes, if any, in manufacturing equipment and processes or materials used.
      The monitoring customer shall be notified of, and may approve modification of the documents listed in subclause 5.4 including PID. In particular:
      — change of base materials,
      — change of chemical products,
      — change of process sequence,
      — change in process parameters,
      — change of equipment.
   2. List of PCBs supplied to this specification by the above mentioned plant during the last 24 months.
   3. One recently manufactured high reliability PCB sample for technological examination. The examination and the tests performed shall be in accordance with the example shown in annex B.

b. Based upon the information received, the result of the technological examination and an investigation of the experiences regarding delivery times and quality of PCBs supplied for space projects, the customer may decide upon one of the following:

   1. If there are no nonconformances, to extend the qualification period by two years and eventually to arrange a control visit to the suppliers' manufacturing plant.
   2. If there are nonconformances, the required corrective action shall be negotiated with the supplier in order to enable maintenance of qualifica-

tion status. This can include additional testing be agreed between customer and supplier and submittal of a new PCB sample.

c. The customer shall audit the qualified PCB lines, as a minimum, every second year.

14.3 Qualification withdrawal

The qualification shall be withdrawn if:

a. The submitted space quality sample is rejected.

b. The materials or manufacturing processes are modified without prior authorization by the customer that has given the qualification approval.

c. The customer has had difficulties in, for example, delivery time and manufacturing defects.

d. Results of an audit at the manufacturing facility are unsatisfactory.

15

Quality assurance for manufacturing

15.1 General

The quality assurance requirements are defined in ECSS-Q-20.

No repair is allowed on finished bare printed boards.

15.2 Data

The quality records (e.g. logbooks) shall be retained for at least ten years or in accordance with project contract requirements, and contain as a minimum the following.

- copy of final inspection documentation;
- nonconformance reports and corrective actions;
- copy of the inspection and test results with reference to, for example, the relevant procedure and personnel.

15.3 Nonconformance

Any nonconformance that has been observed during manufacturing, inspection and testing shall be dispositioned according with the quality assurance requirements of ECSS Q-20-09.

15.4 Incoming inspection of raw materials

Raw materials and semi-finished products shall be selected, inspected and tested (e.g. chemical and physical tests) in accordance with the production flow chart. The supplier shall separate and, and prevent the use of, raw materials and semi-finished products that are awaiting completion of test results.

15.5 Traceability

Traceability shall be maintained throughout the manufacturing process from incoming inspection through manufacturing to final test, including details of test equipment and personnel employed in performing the task.

The supplier's control system shall make it possible to determine, in respect of any lot of PCBs, the history of all raw materials and semi-finished products listed in the production flow chart and the individual process steps mentioned herein, and to verify that the items originate from one production lot. In the case of materials with limited shelf-life, the suppliers control system shall provide for means to

verify the validity of the relevant material for use. The verification and re-certification procedure shall be in accordance with ECSS-Q-70-22.

15.6 Calibration

Each electrical and mechanical manufacturing equipment as well as measuring and reference standard shall be periodically calibrated. Any suspected or actual equipment failure shall be recorded and a nonconformance report shall be made and previous manufacturing results shall be examined to ascertain whether or not a re-inspection or re-testing is required.

15.7 Workmanship standards

Visual standards consisting of photos or drawings of microsections or other visual aids that clearly illustrate the quality characteristics required shall be available to each inspector.

15.8 Inspection

During all stages of the manufacturing the inspection points shall be observed. Quality conformance inspection shall be performed using quality test specimen and microsections.

15.9 Operator and inspector training

All operators and inspectors shall be suitably trained for the their task and for the understanding of the necessary quality assurance requirements.

15.10 Quality test specimen

The supplier shall produce with each panel quality test specimens for in-house quality control purposes and one to be supplied to the customer in accordance with ECSS-Q-70-11A subclause 8.2.

15.11 Microsection

The supplier shall produce with each panel microsections for in-house quality control purposes and one to be supplied to the customer in accordance with ECSS-Q-70-11A subclause 8.3.

15.12 Final inspection and tests

The supplier shall have an in-house procedure for final inspection of PCBs; this shall include visual inspection according to subclause 8.1 and specific dimensional check according to subclause 8.2 and customer requirements.

Electrical testing shall be agreed between customer and supplier in accordance with ECSS-Q-70-11A subclause 8.3.

The quality test specimen representative of the PCB and produced on the same panel shall, as a minimum, be subjected to continuity test, solderability test and thermal stress test. Other specific test can be agreed with the customer.

Microsection of holes as received and after thermal stress tests (rework simulation) shall be performed.

The PCBs shall be cleaned and dried before packaging according to ECSS-Q-70-11A subclause 7.2. The cleanliness values shall be in accordance with ECSS-Q-70-08A subclause 11.3.

16

Quality assurance for delivery

16.1 Packaging

The PCB supplier shall have suitable packaging facilities to conform to the requirements of ECSS-Q-70-11A clause 7.

16.2 Documentation

See ECSS-Q-70-11A subclause 6.2.

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17

Minimum requirements acceptable for high reliability PCBs

17.1 General

The types of PCBs covered by this Standard are:

- Rigid single-sided and double-sided boards:
  - Rigid single-sided and double-sided boards: see subclause 17.2 Table 2,
  - Rigid single-sided and double-sided boards for high frequency application: see subclause 17.2 Table 3.
- Flexible printed boards: see subclause 17.3 Table 4.
- Rigid-flex printed boards: see subclause 17.4 (see 17.3 Table 4 for the flexible part and 17.5 Table 5 for the rigid part).
- Rigid multilayer boards: see subclause 17.5 Table 5.
- Sequential rigid multilayer boards: see subclause 17.6 Table 6.

17.2 Rigid single-sided and double-sided printed boards

These are the minimum requirements acceptable for qualification and procurement of rigid single-sided, double-sided and high frequency PCBs.

Table 2: Limits of approval and characteristics of finished rigid single-sided and double-sided boards

Item	Limits
Base materials	
(according to ECSS-Q-70, IEC specifications and IPC 4101)	- Woven-glass-reinforced epoxy resin FR4 - Woven-glass-reinforced polyimide resin
Dimensional characteristics	
External dimension tolerance	± 0,2 mm
Thickness tolerance	± 10 %
Active board size, maximum	TBD by the supplier
Board thickness maximum	3,2 mm
Positioning tolerance between registration mark and edge of circuit	± 0,2 mm
Conductor width	200 µm minimum (for fine pitch 120 µm width is tolerated if less than 5 mm from component pad)
Spacing between conductors	300 µm minimum (for fine pitch 150 µm spacing is tolerated if less than 5 mm from component pad)
Conductor tolerance (minimum/maximum)	TBD by the supplier, ±20 % maximum
Tolerance on diameter of terminal pads	TBD by the supplier, ±20 % maximum
Minimum hole diameter:	
- component hole	According to ECSS Q-70-08
- via hole	0,25 mm minimum and maximum aspect ratio t/d = 6
Tolerance on diameter of plated-through holes:	
- nominal Ø ≥ 0,7 mm	Δ maximum 0,15 mm for component hole
- nominal Ø < 0,7 mm	Δ maximum 0,20 mm
Tolerance on diameter of non-plated-through holes	Δ maximum 0,20 mm
Positioning tolerance of holes with respect to reference mark	±0,1 mm
Relative misregistration pad/hole	≤ 0,15 mm
Misalignment determined by measuring minimum annular ring:	
- solder side	0,20 mm
- component side (reduced pads)	0,10 mm
- non-soldering hole	0,10 mm
Electrolytic coatings	
Electrolytic copper plating	
- minimum purity	99,5 %
- thickness	
• surface pattern	≥ 25 µm
• plated-through holes	≥ 25 µm
• via holes	≥ 20 µm

Table 2: Limits of approval and characteristics of finished rigid single-sided and double-sided boards *(continued)*

Item	Limits
Tin lead plating after reflow	
– tin content of alloy	(63 ± 8) %
– thickness on surface	8 µm in highest part
– thickness in plated-through holes	8 µm in highest part (minimum half height of hole wall)
– thickness on corner angle	2 µm
Electrolytic gold plating	
– minimum purity	99,8 % (shall not contain more than 0,2 % silver)
– thickness on nickel	(4 ± 3) µm
– thickness on copper	(5 ± 2) µm
Electrolytic nickel plating	Optional under gold
– thickness	2 µm to 10 µm
Mechanical characteristics	
Warp and twist	≤ 1,1 % for board thickness ≥1,6 mm ≤ 1,5 % for board thickness <1,6 mm
Conductor adhesion/peel strength	
– on epoxy	≥ 16 N/cm
– on polyimide	≥ 12 N/cm
Pull strength	
– for terminal pads 4 mm Ø	
• on epoxy	≥ 140 N
• on polyimide	≥ 80 N
– for terminal pads 2 mm Ø	
• on epoxy	≥ 35 N
• on polyimide	≥ 20 N
Electrical characteristics	
Insulation resistance	
– intralayer [a]	> 10^4 MΩ
– interlayer [b]	> 10^5 MΩ
Withstanding voltage per mm spacing between conductors	
– intralayer and interlayer	1 000 V r.m.s.
Short time overload	
– 0,035 mm copper thickness	7 A for 4 s
– 0,070 mm copper thickness	14 A for 4 s
Long time overload, destructive current	
– 0,035 mm copper thickness	I ≥ 8 A
– 0,070 mm copper thickness	I ≥ 16 A

[a] i.e. in the same layer.

[b] i.e. between opposite layers.

Table 3: Limits of approval and characteristics of finished rigid single-sided and double-sided boards for high frequency application

Item	Limits
Base materials	
(according to ECSS-Q-70, IEC specifications and IPC 4101)	– Random-glass-reinforced PTFE resin with or without Al backing – Woven-glass-reinforced PTFE resin – Ceramic filled woven-glass-reinforced PTFE resin – Ceramic filled PTFE resin with or without Al backing – Ceramic filled × linked hydrocarbon/thermo-set polymer – Woven-glass-reinforced epoxy resin FR4 – Quartz filled polyimide resin
Dimensional characteristics	
External dimension tolerance	±0,2 mm
Thickness tolerance	±10 %
Active board size, maximum	TBD by the supplier
Board thickness (minimum/maximum)	TBD by the supplier and customer according to electrical performance
Positioning tolerance between registration mark and edge of circuit	±0,2 mm
Conductor width/spacing	TBD by the supplier and customer according to electrical performance
Tolerance on conductor (minimum/maximum)	TBD by the supplier
Tolerance on diameter of terminal pads	TBD by the supplier and customer according to electrical performance
Minimum hole diameter	
– component hole	According to ECSS Q-70-08
– via hole	0,25 mm minimum and maximum aspect ratio t/d = 6
Tolerance on diameter of plated-through holes	
– nominal Ø ≥ 0,7	Δ maximum 0,15 mm for component hole
– nominal Ø < 0,7	Δ maximum 0,20 mm
Tolerance on diameter of non-plated-through holes	Δ maximum 0,20 mm
Positioning tolerance of holes with respect to reference mark	±0,1 mm
Relative misregistration pad/hole	≤ 0,15 mm
Misalignment determined by measuring minimum annular ring	
– solder side	0,2 mm
– component side (reduced pads)	0,1 mm
– non-soldering hole	0,1 mm

Table 3: Limits of approval and characteristics of finished rigid single-sided and double-sided boards for high frequency application *(continued)*

Item	Limits
Electrolytic coatings	
Electrolytic copper plating	
– minimum purity	99,5 %
– thickness	
• surface pattern for soldering pads	≥ 25 µm (total thickness of basic – plus electrolytic copper ≥ 40 µm)
• plated-through holes	≥ 25 µm
• via hole	≥ 20 µm
Tin lead plating after reflow	
– tin content of alloy	(63 ± 8) %
– thickness on surface	≥ 8 µm in highest part
– thickness in plated-through holes	≥ 8 µm in highest part (minimum half height of hole wall)
– on corner angle	≥ 2 µm
Electrolytic gold plating	
– minimum purity	99,8 % (shall not contain more than 0,2 % silver)
– thickness on nickel	1 µm to 7 µm
Electrolytic nickel plating	Optional under gold
– thickness	2 µm to 10 µm
Mechanical characteristics	
Warp and twist	
– random-glass-reinforced PTFE resin	n.a.
– woven-glass-reinforced PTFE resin	n.a.
– ceramic filled PTFE resin	≤ 1,1 %
– ceramic filled x-linked hydrocarbon/thermoset polymer	≤ 1,1 %
– woven-glass-reinforced epoxy resin FR4	≤ 1,1 % for board thickness ≥1,6 mm ≤ 1,5 % for board thickness <1,6 mm
– quartz filled polyimide	≤ 1,1 % for board thickness ≥1,6 mm ≤ 1,5 % for board thickness <1,6 mm
Conductor adhesion/peel strength	
– on PTFE reinforced/ceramic filled or non-filled	≥ 8 N/cm
– X-linked hydrocarbon	≥ 8 N/cm
– on epoxy	≥ 16 N/cm
– on polyimide quartz	≥ 12 N/cm

Table 3: Limits of approval and characteristics of finished rigid single-sided and double-sided boards for high frequency application *(continued)*

Item	Limits
Pull strength	
– for terminal pads 4 mm Ø on PTFE reinforced/ceramic filled or non-filled	≥ 60 N
• X-linked hydrocarbon	≥ 60 N
• on epoxy	≥ 140 N
• on polyimide quartz	≥ 60 N
– for terminal pads 2 mm Ø on PTFE reinforced /ceramic filled or non-filled	≥ 12 N
• X-linked hydrocarbon	≥ 12 N
• on epoxy	≥ 35 N
• on polyimide quartz	≥ 20 N
Electrical characteristics	
Insulation resistance	
– intralayer	> 10^4 MΩ
– interlayer	> 10^5 MΩ
Withstanding voltage per mm spacing between conductors	
– intralayer and interlayer	1 000 V r.m.s.
Short time overload	
– 0,009 mm copper thickness	n.a.
– 0,017 mm copper thickness	n.a.
– 0,035 mm copper thickness	7 A for 4 s
– 0,070 mm copper thickness	14 A for 4 s
Long time overload, destructive current	
– 0,009 mm copper thickness	n.a.
– 0,017 mm copper thickness	n.a.
– 0,035 mm copper thickness	I ≥ 8 A
– 0,070 mm copper thickness	I ≥ 16 A
Permittivity	TBD by the supplier and customer according to electrical performance
Loss angle Tg δ	TBD by the supplier and customer according to electrical performance

17.3 Flexible printed boards

These are the minimum requirements acceptable for qualification and procurement of flexible PCBs

Table 4: Limits of approval and characteristics of finished flexible printed boards

Item	Limits
Base materials (according to ECSS-Q-70, IEC specifications and IPC 4101)	Flexible copper-clad polyimide film
Dimensional characteristics	
External dimension tolerance	±0,4 mm
Thickness tolerance	±20 %
Active board size, maximum	TBD by the supplier
Board thickness maximum	0,4 mm
Positioning between registration mark and edge of circuit	±0,4 mm
Conductor width/spacing	(250 μm/250 μm) minimum
Conductor tolerance (minimum/maximum)	TBD by the supplier
Tolerance on diameter of terminal pads	TBD by the supplier
Minimum diameter of plated-through holes	0,25 mm
Tolerance on diameter of plated-through holes for components:	
- nominal Ø ≥ 0,7	Δ maximum 0,15 mm
- nominal Ø < 0,7	Δ maximum 0,20 mm
Tolerance on diameter of non-plated-through holes	Δ maximum 0,20 mm
Positioning of holes with respect to reference mark	±0,10 mm
Relative misregistration pad/hole	±0,15 mm
Registration of sides	±0,10 mm
Cutting of insulation coating tolerance	
- internal cutting	±0,50 mm
Misalignment determined by measuring minimum annular ring	
- solder side	0,25 mm
- reduced terminal pads (oblong)	0,10 mm
- non-soldering holes	0,10 mm
Misalignment of insulation coating determined by measuring rest of metal:	
- plated-through holes	0,15 mm
- non-plated-through holes	0,25 mm
Number of layers	2

Table 4: Limits of approval and characteristics of finished flexible printed boards *(continued)*

Item	Limits
Electrolytic coatings	
Electrolytic copper plating	
– minimum purity	99,5 %
– thickness	
• surface pattern	≥ 25 µm
• plated-through holes	≥ 25 µm
Tin lead plating after reflow	
– tin content of alloy	(63 ± 8) %
– thickness on surface	≥ 8 µm in highest part
– thickness in plated-through holes	≥ 8 µm in highest part (minimum half height of hole wall)
– on corner angle	≥ 2 µm
Mechanical characteristics	
Conductor adhesion/peel strength	≥ 10 N/cm
Pull strength	
– for terminal pads 4 mm Ø	≥ 60 N
– for terminal pads 2 mm Ø	≥ 12 N
Resistance to bending cycles	≥ 250 cycles
Bending test for rigid-flex boards	≥ 25 cycles
Electrical characteristics	
Insulation resistance	
– intralayer	≥ 10^4 MΩ
– interlayer	≥ 10^5 MΩ
– with temperature at 80 °C	≥ 10^2 MΩ
Withstanding voltage per mm spacing between conductors	1 000 V r.m.s.
Short time overload	7 A for 4 s
Long time overload, destructive current	≥ 8 A

17.4 Rigid-flex printed boards

For the minimum requirements acceptable for qualification and procurement of rigid-flex PCBs the limits of approval and the characteristics of finished boards shall be in accordance with:

- subclause 17.3 Table 4 for the flexible part,
- subclause 17.5 Table 5 for the rigid part.

For the construction of multilayer rigid-flex the flexible copper clad polyimide film shall be without adhesive

17.5 Rigid multilayer printed boards

These are the minimum requirements acceptable for qualification and procurement of rigid multilayer PCBs.

Table 5: Limits of approval and characteristics of finished rigid multilayer printed boards

Item	Limits
Base materials	
(according to ECSS-Q-70, IEC specifications and IPC 4101)	- Woven-glass-reinforced epoxy resin - Woven-glass-reinforced polyimide resin - Woven-glass-reinforced bismaleimide/trazine modified epoxy (HTg) resin - Non-woven aramide-reinforced polyimide resin
Dimensional characteristics	
External dimension tolerance	±0,2 mm
Thickness tolerance	±10 %
Maximum active board size	TBD by the supplier
Maximum board thickness	3,2 mm
Positioning between registration mark and edge of circuit	±0,2 mm
Conductor width	
- internal	120 µm minimum
- external	200 µm minimum (for fine pitch 120 µm width is tolerated if less than 5 mm from component pad)
Conductor spacing	
- internal	150 µm minimum
- external	300 µm minimum (for fine pitch 150 µm spacing is tolerated if less than 5 mm from component pad)
Conductor tolerance (minimum/maximum)	TBD by the supplier
Tolerance on diameter of terminal pads	TBD by the supplier
Minimum drilled hole diameter	
- component hole	According to ECSS Q-70-08
- via hole	0,25 mm minimum and maximum aspect ratio t/d = 6
Tolerance on diameter of plated-through holes	
- nominal $\varnothing \geq 0,7$	Δ maximum 0,15 mm for component hole
- nominal $\varnothing < 0,7$	Δ maximum 0,20 mm
Tolerance on diameter of non-plated-through holes	Δ maximum 0,20 mm
Positioning of holes with respect to reference mark	±0,1 mm
Relative misregistration pad/hole	≤ 0,15 mm
Misalignment determined by measuring minimum annular ring	
- external layers	
• solder side	0,20 mm
• component side (reduced pads)	0,10 mm
• non-soldering hole	0,10 mm
- internal layers	50 µm

Table 5: Limits of approval and characteristics of finished rigid multilayer printed boards *(continued)*

Item	Limits
Layer to layer registration	±100 µm
Number of layers	18 maximum
Electrolytic coatings	
Electrolytic copper plating	
– minimum purity	99,5 %
– thickness	
• surface pattern	≥ 25 µm
• plated-through holes	≥ 25 µm
• via holes	≥ 20 µm
Tin lead plating after reflow	
– tin content of alloy	(63 ± 8) %
– thickness on surface	≥ 8 µm in highest part
– thickness in plated-through holes	≥ 8 µm in highest part (minimum half height of hole wall)
– on corner angle	≥ 2 µm
Electrolytic gold plating	
– minimum purity	99,8 % (shall not contain more than 0,2 % silver)
– thickness on nickel	(4 ± 3) µm
– thickness on copper	(5 ± 2) µm
Electrolytic nickel plating	Optional under gold
– thickness	2 µm to 10 µm
Insulation between layers	70 µm minimum
Mechanical characteristics	
Warp and twist	≤1,1 % for board thickness ≥ 1,6 mm ≤1,5 % for board thickness < 1,6 mm
Conductor adhesion/peel strength	
– on epoxy with Tg < 160 °C	≥ 16 N/cm
– on epoxy with Tg > 180 °C	≥ 12 N/cm
– on polyimide	≥ 12 N/cm
– on bismaleimide/trazine modified epoxy HTg	≥ 12 N/cm
– aramide/polyimide	≥ 6 N/cm

Table 5: Limits of approval and characteristics of finished rigid multilayer printed boards *(continued)*

Item	Limits
Bond strength/pull strength	
– for terminal pads 4 mm Ø	
• on epoxy Tg < 160 °C	≥ 140 N
• on epoxy Tg > 180 °C	≥ 80 N
• on polyimide	≥ 80 N
• on bismaleimide/trazine modified epoxy HTg	≥ 60 N
• on aramide/polyimide	≥ 60 N
– for terminal pads 2 mm Ø	
• on epoxy Tg < 160 °C	≥ 35 N
• on epoxy Tg > 180 °C	≥ 20 N
• on polyimide	≥ 20 N
• on bismaleimide/trazine modified epoxy HTg	≥ 12 N
• on aramide/polyimide	≥ 12 N
Electrical characteristics	
Insulation resistance	
– intralayer	> 10^4 MΩ
– interlayer	> 10^5 MΩ
Withstanding voltage per mm spacing between conductors	
– intralayer and interlayer	1 000 V r.m.s.
Short time overload	
– 35 μm copper thickness	7 A for 4 s
– 70 μm m copper thickness	14 A for 4 s
Long time overload, destructive current	
– 35 μm copper thickness	I ≥ 8 A
– 70 μm copper thickness	I ≥ 16 A
Internal short circuit	
– insulation resistance	≥ 10^3 MΩ

17.6 Sequential rigid multilayer printed boards

These are the minimum requirements acceptable for qualification and procurement of sequential rigid multilayer PCBs.

Table 6: Limits of approval and characteristics of finished sequential rigid multilayer printed boards

Item	Limits
Base materials	
(according to ECSS-Q-70, IEC specifications and IPC 4101)	– Woven-glass-reinforced epoxy resin – Woven-glass-reinforced polyimide resin – Woven-glass-reinforced bismaleimide/trazine modified epoxy (HTg) resin – Non-woven-aramide-reinforced polyimide resin
Dimensional characteristics	
External dimension tolerance	±0,2 mm
Thickness tolerance	±10 %
Maximum active board size	TBD by the supplier
Maximum board thickness	3,2 mm
Positioning between registration mark and edge of circuit	Δ maximum 0,20 mm
Conductor width	
– internal	120 µm minimum
– external	200 µm minimum (for fine pitch 120 µm width is tolerated if less than 5 mm from component pad)
conductor spacing	
– internal	150 µm minimum
– external	300 µm minimum (for fine pitch 150 µm spacing is tolerated if less than 5 mm from component pad)
Conductor tolerance (minimum/maximum)	TBD by the supplier
Tolerance on diameter of terminal pads	TBD by the supplier
Minimum drilled hole diameter	
– component hole	According to ECSS Q-70-08
– via hole	0,25 mm minimum and maximum aspect ratio t/d = 6
– buried via	TBD by the supplier maximum aspect ratio t/d = 6
– blind via produced sequentially	TBD by the supplier maximum aspect ratio t/d = 6
Tolerance on diameter of plated-through holes	
– nominal Ø ≥ 0,7	Δ maximum 0,15 mm for component hole
– nominal Ø < 0,7	Δ maximum 0,20 mm
Tolerance on diameter of non-plated-through holes	Δ maximum 0,20 mm
Positioning of holes with respect to reference mark	±0,10 mm
Relative misregistration pad/hole	≤ 0,15 mm

Table 6: Limits of approval and characteristics of finished sequential rigid multilayer printed boards *(continued)*

Item	Limits
Misalignment determined by measuring minimum annular ring	
– external layers	
• solder side	0,20 mm
• component side (reduced pads)	0,10 mm
• non-soldering hole	0,10 mm
– internal layers	0,05 mm
Layer to layer registration	±100 µm
Number of layers	18 maximum
Electrolytic coatings	
Electrolytic copper plating	
– minimum purity	99,5 %
– thickness	
• surface pattern	≥ 25 µm
• plated-through holes	≥ 25 µm
• via holes	≥ 20 µm
• buried via holes	≥ 18 µm
• blind via holes	≥ 18 µm
Tin lead plating after reflow	
– tin content of alloy	(63 ± 8) %
– thickness on surface	≥ 8 µm in highest part
– thickness in plated-through holes	≥ 8 µm highest part (minimum half height of hole wall)
– on corner angle	≥ 2 µm
Electrolytic gold plating	
– minimum purity	99,8 % (shall not contain more than 0,2 % silver)
– thickness on nickel	(4 ± 3) µm
– thickness on copper	(5 ± 2) µm
Electrolytic nickel plating	Optional under gold
– thickness	2 µm to 10 µm
Resin fill in buried vias	see 9.3.3.3 b. 6.
Insulation between layers	70 µm minimum

Table 6: Limits of approval and characteristics of finished sequential rigid multilayer printed boards *(continued)*

Item	Limits
Mechanical characteristics	
Warp and twist	≤ 1,1 % for board thickness ≥ 1,6 mm ≤ 1,5 % for board thickness < 1,6 mm
Conductor adhesion/peel strength	
– on epoxy with Tg < 160 °C	≥ 16 N/cm
– on epoxy with Tg > 180 °C	≥ 12 N/cm
– on polyimide	≥ 12 N/cm
– on bismaleimide/trazine modified epoxy HTg	≥ 12 N/cm
– aramide/polyimide	≥ 6 N/cm
Bond strength/pull strength	
– for terminal pads 4 mm Ø	
• on epoxy Tg < 160 °C	≥ 140 N
• on epoxy Tg > 180 °C	≥ 80 N
• on polyimide	≥ 80 N
• on bismaleimide/trazine modified epoxy HTg	≥ 60 N
• on aramide/polyimide	≥ 60 N
– for terminal pads 2 mm Ø	
• on epoxy Tg < 160 °C	≥ 35 N
• on epoxy Tg > 180 °C	≥ 20 N
• on polyimide	≥ 20 N
• on bismaleimide/trazine modified epoxy HTg	≥ 12 N
• aramide/polyimide	≥ 12 N
Electrical characteristics	
Insulation resistance	
– intralayer	> 10^4 MΩ
– interlayer	> 10^5 MΩ
Withstanding voltage per mm spacing between conductors	
– intralayer and interlayer	1 000 V r.m.s.
Short time overload	
– 0,035 mm copper thickness	7 A for 4 s
– 0,070 mm copper thickness	14 A for 4 s
Long time overload, destructive current	
– 0,035 mm copper thickness	I ≥ 8 A
– 0,070 mm copper thickness	I ≥ 16 A
Internal short circuit	
– insulation resistance	≥ 10^3 MΩ

Annex A (informative)

Index of test descriptions

Annex B (informative)

Example of evaluation test report

Metallurgical inspection of printed circuit board	**Report no.:**
Description and history of sample:	
Project and cost code number:	
Date:	**Originator:** / **Telephone:**

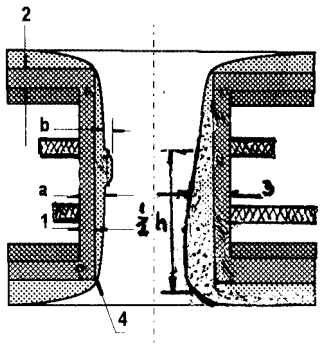
Visual Inspection Parameters
Minor defects (m) and major defects (M) are circled if found

1.	**Conductive pattern**	
1.1	Short circuits	M
1.2	Open circuits	M
1.3	Edge roughness of conductors exceeding 20 % of tolerance	M
1.4	Reduction of conductor exceeding 20 %	M
1.5	Scratches exposing copper plate	M
1.6	Superficial scratches	m
1.7	Isolated peaks or dwells < 20 % of width	m
1.8	Dewetting on solderable zones	M
1.9	Dewetting on edges of mass zones	m
1.10	Undercut exceeding total copper thickness	M
1.11	Spacing between conductors < 0,3 mm	M
2.	**Base laminate**	
2.1	Imbedded foreign particle	M
2.2	Delamination	M
2.3	Cracks visible to naked eye	M
2.4	Roughness of board edges > 0,1 mm per 10 mm	M
2.5	Warp and twist (PCB ≥ 1,6 mm) > 1,1 %	M
2.6	Warp and twist (PCB < 1,6 mm) > 1,5 %	M
2.7	Tolerance not exceeding 25 %	m
2.8	Pits and dents	M
2.9	Chipping	M
3.	**Holes**	
3.1	Open circuits, cracks	M
3.2	Hole positions ±0,01 mm	
3.3	Ratio pad diameter-hole diameter smaller than specified	mM
3.4	Eccentricity	m
3.5	Dirt, not removable	M
4.1	**Identification impossible**	M
5.	**Dimensions**	
5.1	External dimensions: ±0,2 mm	
5.2	Tolerance of plated-through holes:	
	Holes ≥ 0,7 mm: Δ max. 0,15 mm	
	Holes < 0,7 mm: Δ max. 0,20 mm	
	Remarks	

6. Peel strength (requirement 16 N/cm)

7. Solderability

8. Microsection mount numbers

Measurement on microsection		**Required**	**Measured**	**Remarks**
	1. Copper in PTH	minimum 25 µm		OK/NOK
	2. Cu at surface pattern	minimum 25 µm		OK/NOK
	3. Sn/Pb in hole	minimum 8 µm		OK/NOK
	3. Sn/Pb on pad	minimum 8 µm		OK/NOK
	4. Sn/Pb in angle area	minimum 2 µm		OK/NOK
	5. Internal bulging	b<a		OK/NOK

Conclusions:

Inspected date:	**Approved date:**	**Distribution:**

Annex C (informative)

Example of check-list

Materials and Processes Division

Metallic Materials and Processes Section

Division Matériaux et Procédés

Section Matériaux & Procédés Métalliques

Check-list for double sided and multilayer printed circuit board fabrication facilities

Full name of company:
Address of company:
Town:
Country:
Phone:
Fax:

Date(s) of audit	
Name of auditor(s)	**Signature of auditor(s)**

Check-list for double and multilayer printed circuit board fabrication facilities		
Process or inspection step	**Presented in documentation**	**Details and remarks**
1. Incoming inspection of laminates • Peel strength • Visual criteria • Solderability • Etchability • Warp and twist		
2. Prepreg controls (MLB) • Gel time • Resin flow • Resin content • Volatile content		
3. Inspection of artwork • Touch up • Control		
4. Photo-resist • Cleaning • Application • Exposure • Development		

Check-list for double and multilayer printed circuit board fabrication facilities		
Process or inspection step	**Presented in documentation**	**Details and remarks**
5. Inspection		
6. Etching process		
7. Resist stripping process		
8. Inspect etching		
9. Pre-lamination cleaning (MLB)		
10. Cutting and laying of prepreg (MLB)		

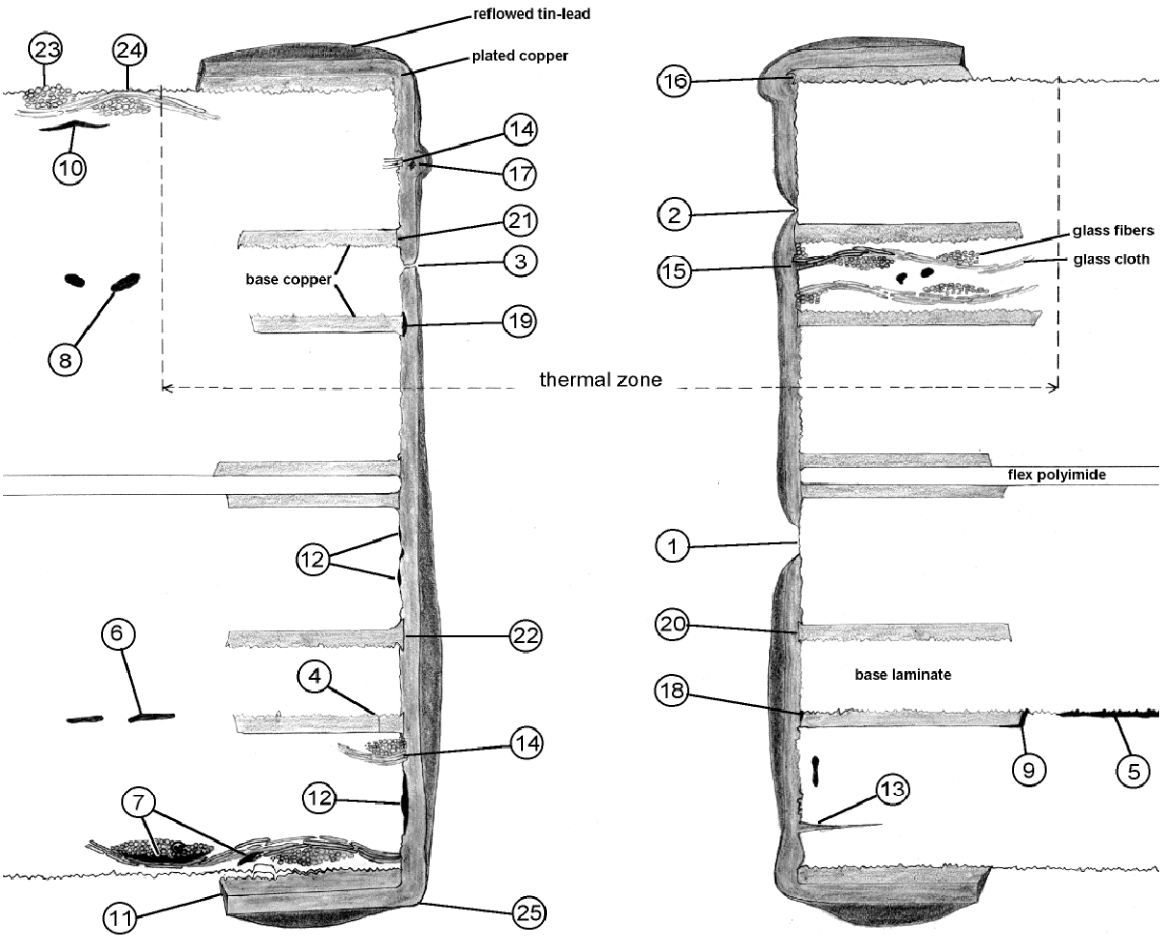
Check-list for double and multilayer printed circuit board fabrication facilities		
Process or inspection step	**Presented in documentation**	**Details and remarks**
11. Inspect pre-lamination (MLB)		
12. Laminate process (MLB)		
13. Inspect drill tools		
14. Drilling and cleaning		
15. Inspect end item		
16. Etchback (MLB) - Desmear		
17. Inspect etchback		

Check-list for double and multilayer printed circuit board fabrication facilities		
Process or inspection step	**Presented in documentation**	**Details and remarks**
18. Electroless copper plating and bath control		
19. Copper plate and bath control		
20. Microsection/Inspection		
21. Tin-lead plating and bath control		
22. Microsection and controls		
23. Additional platings Ni, Au, Rh, and controls		
24. Tin-lead fusing operation		

Check-list for double and multilayer printed circuit board fabrication facilities		
Process or inspection step	**Presented in documentation**	**Details and remarks**
25. Routing of PCBs		
26. Final microsection		
27. Inspect end item		
28. Clean periodic test for ionic contamination		
29. Packaging		
30. Other comments		

Annex D (informative)

Example of plated-through hole microsection



Cross section of a flex-rigid multilayer plated-through hole with typical freatures and defects

1 - plating void
2 - pinhole
3 - plating crack
4 - foil crack
5 - delamination
6 - blistering
7 - measling
8 - laminate void (out of thermal zone)
9 - resin recession innerlayer
10 - resin crack
11 - lifted land
12 - resin recession
13 - wicking (copper)
14 - glass firbre protrusion
15 - rough drilling and wicking (copper)
16 - burr
17 - plating nodule
18 - interplane inclusion (smearing)
19 - interplace separation
20 - positive etch back (inner layer copper imbedded in plated copper)
21 - negative etch back
22 - nailheading
23 - weave exposure (fibres visible)
24 - weave texture (glass cloth shape visible)
25 - tin lead thichness $< 1\mu$ in angles

Figure 32: Example of plated-through hole microsection

Bibliography

IEC 60068-1 (1988-06)	Environmental testing. Part 1: General and guidance
IEC 60194 (1999-04)	Printed board design, manufacture and assembly — Terms and definitions
IEC 61249 series	Materials for printed boards and other interconnection structures
IEC 60249 series	Base materials for printed circuits
IPC-MF-150F	Metal foil for printed wiring applications
IPC-CF-152B	Composite metallic material specification for printed wiring board

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ECSS Document Improvement Proposal

1. Document I.D.	2. Document date	3. Document title
ECSS-Q-70-10A	23 November 2001	Qualification of printed circuit boards

4. Recommended improvement (identify clauses, subclauses and include modified text or graphic, attach pages as necessary)

5. Reason for recommendation

6. Originator of recommendation

Name:	Organization:	
Address:	Phone: Fax: e-mail:	**7. Date of submission:**

8. Send to ECSS Secretariat

Name:	Address:	Phone: +31-71-565-3952
W. Kriedte	ESTEC, P.O. Box 299	Fax: +31-71-565-6839
ESA-TOS/QR	2200 AG Noordwijk	e-mail: Werner.Kriedte@esa.int
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Note: The originator of the submission should complete items 4, 5, 6 and 7.

This form is available as a Word and Wordperfect-file on internet under
http://www.estec.esa.nl/ecss

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